INSTRUCTION MANUAL

EMR MODEL 2745
DATA DISTRIBUTOR
(REVISION A)

EMR TELEMETRY DIVISION
BOX 3041 • SARASOTA, FLORIDA

INSTRUCTION MANUAL

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DATA DISTRIBUTOR
(REVISION A)

EMR TELEMETRY
BOX 3041 • SARASOTA, FLORIDA 33578

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual describes the EMR Model 2745 Data Distributor. The unit accepts parallel multiplex data (up to 16 bits) with synchronizing pulses from an EMR 2710 PAM-PDM Signal Conditioner, EMR 2730 or 2731 PCM Frame Synchronizer, EMR 2735 or 2736 Subframe Synchronizer, EMR 2746 PCM Decommutator or similar interface equipment and provides by patchboard selection, channel transfer pulses (up to 32) for entering selected channels into an EMR 2750 Digital-to-Analog Converter or other compatible readout device. Any one of the 32 channels can be displayed on the data distributor front panel in 16-bit parallel form.

NOTE

All references in this section to the Model 2730 PCM Frame Synchronizer are also applicable to the Model 2731 PCM Frame Synchronizer. All references to the Model 2735 PCM Subframe Synchronizer apply to the Model 2736 PCM Subframe Synchronizer.

1.2 FUNCTIONAL DESCRIPTION

1.2.1 Automated Data-Processing System Relationship

The Model 2745 is one of the EMR Modular Telemetry Processor (MTP) units which form the telemetry interface for an automated telemetry-processing system. The Model 2745 is a complete subsystem, with power supply, programmable patchboard, input/output connectors, and internal cooling. The unit can be used as part of a simple, independent decommutator or can be used for quick-look displays in a computer-controlled data processing system.

A typical system using the Model 2745 is shown in Figure 1-1. In this system, the incoming serial pulse-code-modulated (PCM) pulse train is recovered from data link noise and perturbations by the EMR Model 2721 PCM Signal Conditioner and bit synchronization (0° and 90° bit rate clocks) is established. The EMR Model 2730 Frame Synchronizer and the EMR Model 2735 Subframe Synchronizer perform frame and subframe synchronization and serial-to-parallel conversion of the serial PCM pulse train. The parallel data and synchronization pulses are routed to the EMR Model 6130 Computer and to the Model 2745 Data Distributor.

The Model 2745, in conjunction with the Model 2750 Digital-to-Analog Converter, provides immediate quick-look display of selected data channels before entry into the Model 6130 Computer. Selected, processed data channels can also be converted to analog form by direct interface with the computer.

The EMR Model 2790 Signal Simulator and the EMR Model 2791 Perturbation Generator provide data and control signals for system setup, checkout and diagnostic tests. The EMR Model 6130 Computer can control the entire system, or the modular units can be programmed manually.

1.2.2 Functional Relationships

The overall function of the EMR 2745 Data Distributor is to accept a parallel binary data multiplex (16 bits maximum), together with synchronizing pulses, and provide up to 32 channel transfer pulses for specific words in the multiplex by patchboard selection. Figure 1-2 is a simplified block diagram which illustrates the manner in which this overall function is performed. Such a decommutating function enables selected channels to be readily accepted by digital-to-analog converters and other display and storage devices.

1.2.2.1 Input Selection

Any one of three parallel data sources can be selected by a front-panel switch on the data distributor. Sources include outputs from the EMR 2710 PAM-PDM Signal Conditioner, EMR 2730/2735 PCM Frame and Subframe Synchronizers, and the EMR 2746 PCM Decommutator (a portable unit with limited display capability). In addition to the data multiplex, the data distributor requires syllable, word, and frame rate pulses, and subframe increment and reset pulses, according to the data format and source. The data multiplex is routed directly to the data distributor patchboard, and the synchronizing pulses are routed to syllable, word, and frame counters as applicable.

1.2.2.2 Syllable, Word, and Frame Counters

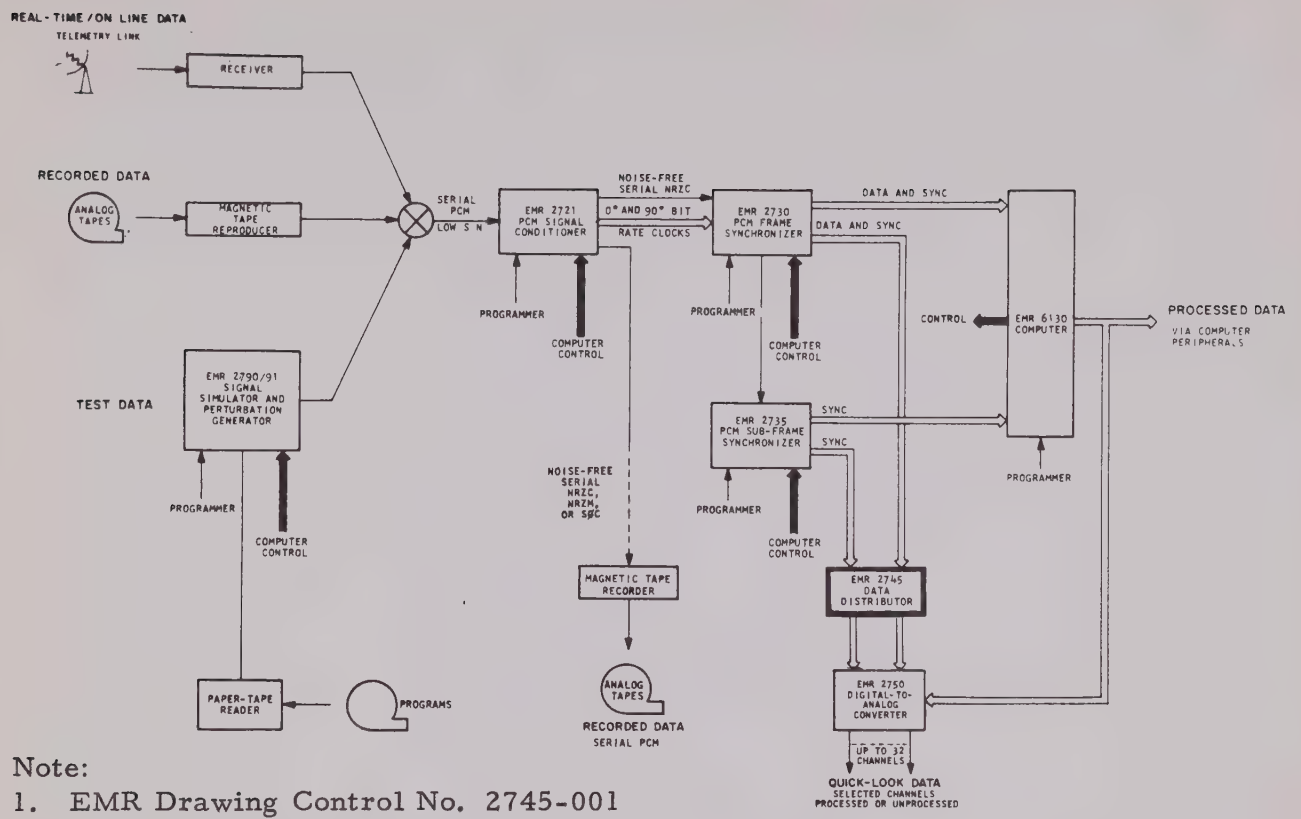
These counters are unitary counters which translate the sync pulses into convenient units, tens, and hundreds counts for further translation into required channel transfer pulses via the patchboard and collection gates.

1.2.2.3 Patchboard

An 18 x 34-hole removable patchboard is located inside the drawer, and is accessible via a hinged panel in the top cover. The patchboard can be programmed to provide a flexible matrix for selecting any required syllable, word and frame count for entry into the collection gates, so that when the selected count occurs, a channel transfer pulse is available as an output from the collection gates. Up to 32 different words or syllables in a frame can be selected in this manner, and the 32 channel transfer output lines are wired to the patchboard for routing flexibility.

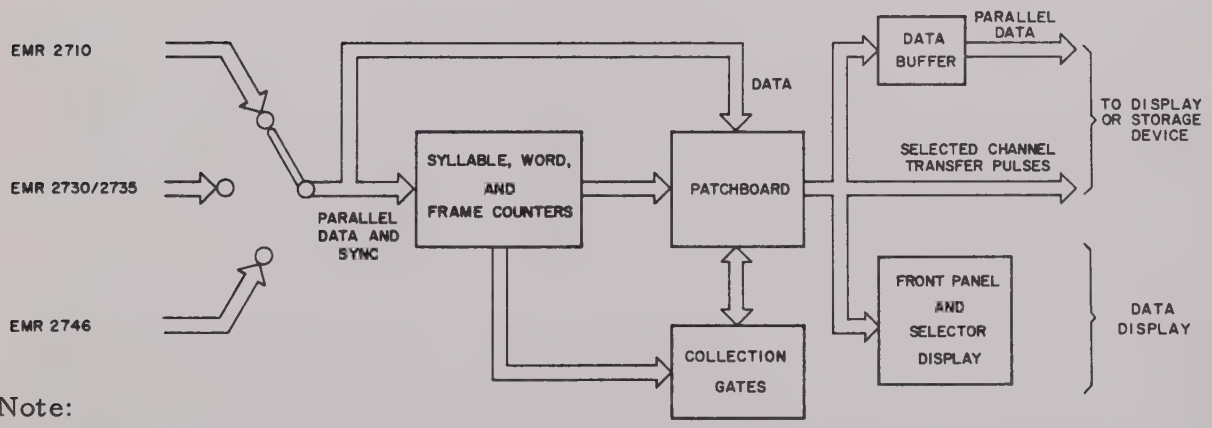
Word selection can be made from formats containing 512 words per frame maximum, and two subframes of 512 frames maximum. Syllable selection can be made from words containing up to 4 syllables maximum.

The channel transfer pulses are routed from the patchboard to an external display or storage device, for selection of the proper parallel data from the data buffer stages. The parallel data is also routed to the data distributor front panel display circuit for selection by the DISPLAY SELECT switches.



Note:
1. EMR Drawing Control No. 2745-001

Figure 1-1. Relationship of EMR Model 2745 to Automated Telemetry System



Note:
1. EMR Drawing Control No. 2745-002

Figure 1-2. Model 2745 Data Distributor, Simplified Functional Block Diagram

1.3 PHYSICAL DESCRIPTION

The standard Model 2745 Data Distributor is a self-contained unit designed for mounting in an Electronic Industries Association (EIA) rack. The front panel of the Model 2745 is 5-1/4 inches by 19 inches. The major subassemblies of the unit are illustrated in Figure 1-3 and described in Table 1-1.

Most of the electrical components contained in the Data Distributor are mounted on printed-circuit cards which plug into card file assembly A1 (Table 1-1). Card file assembly A1 consists of 50 sets of 40-pin connectors. The printed-circuit cards used are listed in Table 1-2. Figure 4-7 is the card file layout which illustrates card locations in card file assembly A1, the circuits used on each card, the logic function of each circuit, and the logic diagram figure number for each logic function.

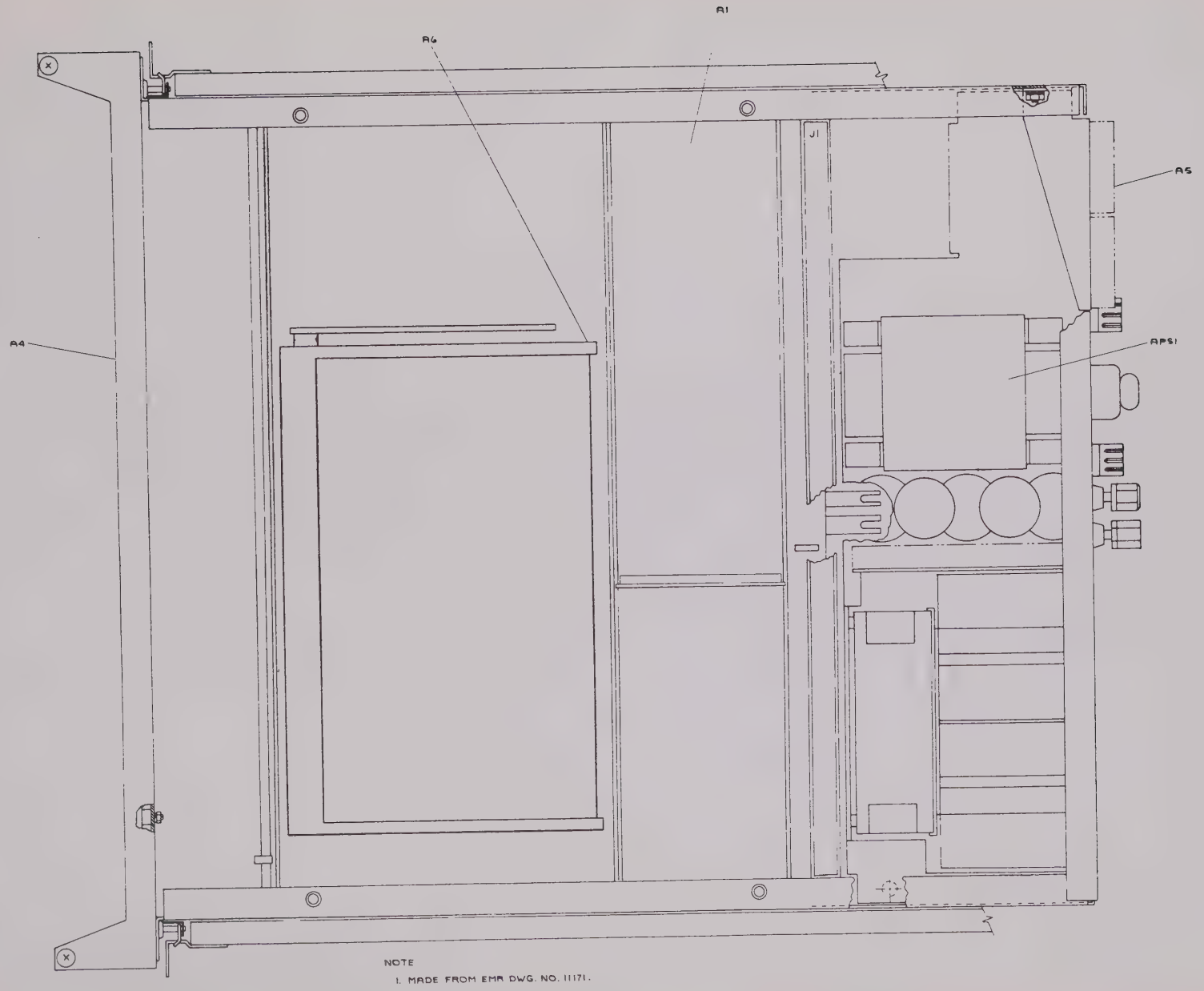


Figure 1-3. Major Subassemblies (Ref. Table 1-1)

Table 1-1. Model 2745, List of Major Subassemblies
(See Figure 1-3)

REF. DESIG.	NAME	FUNCTION
A1	Card File	Provides mounting for printed-circuit logic cards. For a complete description of the logic cards, refer to Section 7 of this manual.
A4	Front Panel	Provides mounting for all front panel controls and displays. A description of the front panel controls and indicators is furnished in Section 3 of this manual.
A5	Connector Assembly	Contains connectors for mating of wiring between the Model 2745 and peripheral equipment. For wiring information, see Figure 3-1 and Tables 3-2 through 3-9.
A6	Patchboard Receiver Assembly	Houses patchboard used to program data distributor outputs.
PS1	EMR Model 2650	Supplies DC voltages for drawer operation. For a complete description of the power supply, refer to EMR Model 2650 Power Supply Instruction Manual.

Table 1-2. List of Printed-Circuit Cards Used in Data Distributor

CARD NO.	ASS'Y NO.	QTY. USED	CARD NOMENCLATURE
2501	4001	6	16-Inverter NAND Gates
2502	4002	1	16-Inverter NAND Buffer Gates
2503	4003	4	12-2 Input NAND Gates
2506	4006	8	Four 8-Input NAND Gates
2546	4046	2	Two 4-Bit Storage Registers
2564	4064	1	Four Gated One Shots
2567	4067	9	One 8-to-10 Bit Shift Register/B
8301	8301	1	Resistor Card Assembly

SECTION 2

SPECIFICATIONS AND MODEL IDENTIFICATION

2.1 GENERAL

This section contains the electrical, mechanical, environmental specifications and model identification information for the Model 2745 Data Distributor.

2.2 ELECTRICAL SPECIFICATION

2.2.1 Inputs

a. Compatible Units: EMR 2710 PAD-PDM Signal Conditioner, EMR 2730/2731 PCM Frame Synchronizers, EMR 2735/2736 PCM Subframe Synchronizers, and EMR 2746 PCM Decommutator.

b. Data Mode: Parallel binary (MSB or LSB aligned).

c. Data Format: Syllable (Byte) Length: one to 16 bits.
Word Length: one to four syllables (bytes).
Frame Length: two to 512 words per frame (four to 2048 syllables).
Subframe Length: two to 512 frames per subframe (ID and recycle).

d. Data Rate: 250 KHz for eight-bit words.

e. Synchronizing Pulses: Syllable, word, and frame rate pulses. Recycle-and ID-subframe-synchronizer increment and reset pulses.

2.2.2 Programming

a. Method: Manual, by removable patchboard (18x34-hole matrix).

b. Identification: Decimal numbering, colored input-output areas, and function titles.

c. Syllable and Word Selection: Syllables: one to four of any word.
Frame Word: one to 512.
Subframe Word: one to 512.

d. Transfer-Pulse Generation: Frame Syllables or Words: Up to 32 maximum.
Subframe Syllables or Words: Up to 31 maximum.
Strapping/Supercommutation: Any number of outputs from two up to 32.

e. LSB/MSB Alignment: 16 bits, maximum.

2.2.3 Outputs

a. Data: 16-bit parallel multiplex MSB/LSB aligned. Data bits may also be aligned in any desired sequence.

b. Channel-Transfer Pulses: 32 individual lines, active as programmed. Pulses on each line are synchronous with the occurrence of a selected syllable/byte/word in the output data multiplex.

2.2.4 Controls and Displays

a. Input: Rotary switch to select any one of three compatible data sources: EMR 2710, EMR 2730/2735, 2731/2736, or EMR 2746.

b. Data Display: 16-bit display.

c. Display Select: Two rotary switches to select any one of the 32 programmed channels for the binary data display.

d. Power: Lighted pushbutton to control and indicate application of the primary power.

e. Lamp Test: Pushbutton to test all data display lamps.

2.2.5 Input and Output Logic Levels

a. Input Voltage: Logic ZERO : 0 to +0.45V DC.
Logic ONE : +3 to +5V DC.

b. Input Current: 1.66ma, maximum, out: V_{in} = 0V.
0.1ma, maximum, in: V_{in} = +5V.

c. Noise Immunity: 0 to +1.1V is recognized as a logic ZERO.
+1.9 to +5V is recognized as a logic ONE.

d. Output Voltage: Logic ZERO : 0 to +0.45V DC.
Logic ONE : +3 to +5V DC.

e. Output Current: The output can sink 8.3ma, maximum V_{out} = 0V.
The output can supply 0.5ma, maximum, V_{out} = +3V.

f. Output Rise and Fall Times: 12 nanoseconds, maximum (measured with maximum load at the output connector).

2.2.6 Power Requirement

a. Voltage:

1. 115V or 120 V RMS, ±10%, 47 to 65 Hz, for Model 2745-01.
2. 115 V or 120V RMS, ±10%, 360 to 440 Hz for Model 2745-71.
3. 230 V ±10%, 47 to 53 Hz for Model 2745-81.

b. Power: 61 watts at 120V.

2.3 MECHANICAL SPECIFICATIONS

a. Panel Size: 5-1/4 in. H by 19 in. W (13.3 by 48.2 cm).

b. Overall Depth: 22 in. (55.9 cm), excluding projections from front panel.

c. Weight: Net 56 pounds (25.4 kg). Shipping, 71 pounds (32.2 kg).

d. Panel Finish: A combination of light and dark green semigloss baking enamel with white lettering is standard. Other panel and lettering paints are available.

e. Mounting: Slides and hardware for installation in an EIA-type rack can be provided.

2.4 ENVIRONMENTAL SPECIFICATIONS

a. Temperature: Operating, $0^{\circ}C$ to $+50^{\circ}C$. Nonoperating, $-40^{\circ}C$ to $+85^{\circ}C$.

b. Shock: Nonoperating, 20g for 10 milliseconds per MIL-STD-810A. Method 516, Procedure I.

c. Vibration: Nonoperating, per MIL-STD-810A. Method 514, Equipment Class 6, Figure 514-6, Curve A.

d. Altitude: Sea level to 10,000 feet.

e. Relative Humidity: 5% to 95%.

2.5 MODEL NUMBER IDENTIFICATION

Specify "Model 2745-$\overset{a}{xx}$-$\overset{b}{x}$-* Data Distributor."

a. Design Sequence:

1. 01 is standard operating from 115 V or 120 V RMS, 47 to 65 Hz, single phase.
2. 71 operates from 115 V or 120 V RMS, 360 to 440 Hz.
3. 81 operates from 230 V, 47 to 53 Hz.

b. Slides (0 = none; 1 = nontilting, nonretracting ChassisTrak; 2 = nontilting, retracting Chassis-Trak; 3 = tilting, nonretracting Chassis-Trak; 4 = tilting, retracting Chassis-Trak; 5 = nontilting, nonretracting Jonathan; 6 = nontilting, retracting Jonathan; 7 = tilting, nonretracting Jonathan; 8 = tilting, retracting Jonathan).

Additional programming patchboards can be supplied.

*Panel paint and lettering codes (00048-00049W = light green panel with dark green withdrawal bar and white lettering; other paint schemes are available on special order).

SECTION 3

INSTALLATION AND OPERATION

3.1 INSTALLATION

The Model 2745 Data Distributor is shipped completely assembled and ready for mounting. Any shortage or damage to the unit should be reported in accordance with the instructions of the EMR Purchase Order Acknowledgment (POA).

The unit is designed for mounting in a standard EIA-type rack, 22 inches deep. The modular unit, which contains a power supply and cooling fan, can be set in an assigned position in an EIA rack or can be placed external to the rack.

The data distributor may be ordered with or without mounting slides. Units without slides are bolted directly to the rack using hardware provided for this purpose. Units equipped with slides are mounted as follows. After unpacking the unit, remove the mounting slides from the unit and mount the slides to the internal frame of the rack. Mounting hardware for this installation is supplied with each unit. Insert the unit into the slides until the unit is firmly seated. The turn-to-lock catches on both sides of the front panel secure each unit in the rack.

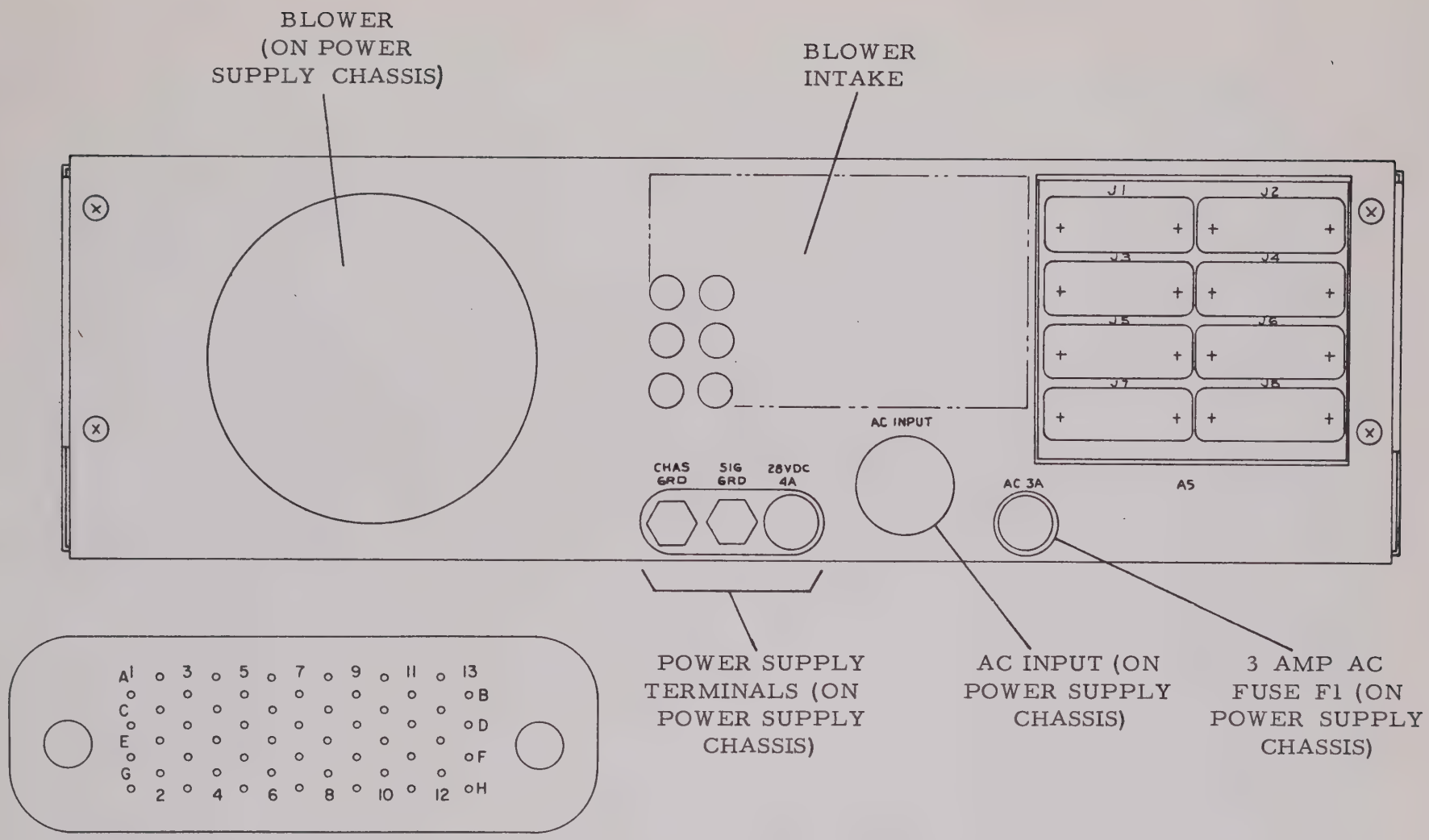
The data distributor may be extended from the rack for servicing by loosening the two front panel turn-to-lock catches and pulling the unit straight out. Push-button stop latches are provided on the outside surfaces of both slides which hold the unit at maximum extension. At this point, the unit may be removed by de-pressing the pushbutton stop latches and pulling the unit straight out.

All external connections are made at the rear of the Model 2745. A six-foot power cable and mating plugs are supplied with the unit. AC power is supplied through the three-pronged, twist-type connector. Data and synchronization input and output connections are made through the eight 52-pin connectors mounted on connector assembly A5 at the rear of the unit. The rear connectors and other rear panel components for the data distributor are illustrated in Figure 3-1 and described in Table 3-1. Pin function listings for connectors J1 through J8 on connector assembly A5 are provided in Tables 3-2 through 3-9.

3.2 PATCHBOARD PROGRAMMING

3.2.1 Patchboard Configuration

The data distributor patchboard configuration is illustrated in Figure 3-2. The outputs of the data distributor syllable, word and frame counters are brought out to the upper (red) portion of the patchboard. Each counter output is capable of driving 11 loads. In the event that more driving capability is required, connections to ten double-inverting BUFFERS are available at the bottom of the patchboard.



PIN LOCATIONS FOR CONNECTORS
A5J1 THROUGH A5J8

NOTE:

1. EMR DRAWING NO. 2745-003

Figure 3-1. Rear Panel Configuration

Table 3-1. Function of Rear Panel Connectors on Data Distributor

REFERENCE DESIGNATION	CONNECTOR TYPE	FUNCTION
A5J1	52-pin	Provides connections for signal inputs from Model 2710 PAM-PDM Signal Conditioner.
A5J2	52-pin	Provides connections for signal inputs from Model 2730 or 2731 PCM Frame Synchronizer.
A5J3	52-pin	Provides connections for signal inputs from Model 2735 or 2736 PCM Subframe Synchronizer.
A5J4	52-pin	Provides connections for signal inputs from Model 2746 PCM Decommutator. (710)
A5J5 through A5J8	52-pin	Provides connections for signal outputs to peripheral equipment.

Table 3-2. Signal Identification for Rear Panel Connector A5J1 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J1	A2	PD01	Parallel data output bits 1 through 12. from EMR 2710
A5J1	B1	GRD	
A5J1	A4	PD02	
A5J1	B3	GRD	
A5J1	A6	PD03	
A5J1	B5	GRD	
A5J1	A8	PD04	
A5J1	B7	GRD	
A5J1	A10	PD05	
A5J1	B9	GRD	
A5J1	A12	PD06	
A5J1	B11	GRD	
A5J1	D13	PD07	
A5J1	B13	GRD	
A5J1	C2	PD08	
A5J1	D1	GRD	
A5J1	C4	PD09	
A5J1	D3	GRD	
A5J1	C6	PD010	
A5J1	D5	GRD	
A5J1	C8	PD011	
A5J1	D7	GRD	
A5J1	C10	PD012	
A5J1	D9	GRD	
A5J1	C12	Spare	
A5J1	D11	Spare	
A5J1	E2	Spare	
A5J1	F1	Spare	

Table 3-2 (Cont'd.). Signal Identification for Rear Panel Connector A5J1 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J1	E4	Spare	
A5J1	F3	Spare	
A5J1	E6	Spare	
A5J1	F5	Spare	
A5J1	E8	OUT DRQ	Output data request.
A5J1	F7	GRD	
A5J1	E10	Spare	
A5J1	F9	Spare	
A5J1	E12	FRATE	Frame rate pulse.
A5J1	F11	GRD	
A5J1	H13	Spare	
A5J1	F13	Spare	
A5J1	G2	Spare	
A5J1	H1	Spare	
A5J1	G4	Spare	
A5J1	H3	Spare	
A5J1	G6	Spare	
A5J1	H5	Spare	
A5J1	G8	Spare	
A5J1	H7	Spare	
A5J1	G10	Spare	
A5J1	H9	Spare	
A5J1	G12	Spare	
A5J1	H11	Spare	

Table 3-3. Signal Identification for Rear Panel Connector A5J2 (Ref. Figure 3-1)

CONNECTOR	PIN		
A5J2	A2	PD01	
A5J2	B1	GRD	
A5J2	A4	PD02	
A5J2	B3	GRD	
A5J2	A6	PD03	
A5J2	B5	GRD	
A5J2	A8	PD04	
A5J2	B7	GRD	
A5J2	A10	PD05	
A5J2	B9	GRD	
A5J2	A12	PD06	
A5J2	B11	GRD	
A5J2	D13	PD07	Parallel data input ~~output~~ bits 1 through 14. from EMR 2730
A5J2	B13	GRD	
A5J2	C2	PD08	
A5J2	D1	GRD	
A5J2	C4	PD09	
A5J2	D3	GRD	
A5J2	C6	PD010	
A5J2	D5	GRD	
A5J2	C8	PD011	
A5J2	D7	GRD	
A5J2	C10	PD012	
A5J2	D9	GRD	
A5J2	C12	PD013	
A5J2	D11	GRD	
A5J2	E2	PD014	
A5J2	F1	GRD	

Table 3-3 (Cont'd.). Signal Identification for Rear Panel Connector A5J2 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J2	E4	PD015	Parallel data ~~output~~ input bits 15 and 16. from EMR 2730
A5J2	F3	GRD	
A5J2	E6	PD016	
A5J2	F5	GRD	
A5J2	E8	Spare	
A5J2	F7	Spare	
A5J2	E10	Spare	
A5J2	F9	Spare	
A5J2	E12	FRATE	Frame rate pulse.
A5J2	F11	GRD	
A5J2	H13	SYRATE	Syllable rate pulse.
A5J2	F13	GRD	
A5J2	G2	WDRATE	Word rate pulse.
A5J2	H1	GRD	
A5J2	G4	Spare	
A5J2	H3	Spare	
A5J2	G6	Spare	
A5J2	H5	Spare	
A5J2	G8	Spare	
A5J2	H7	Spare	
A5J2	G10	Spare	
A5J2	H9	Spare	
A5J2	G12	Spare	
A5J2	H11	Spare	

Table 3-4. Signal Identification for Rear Panel Connector A5J3 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J3	A2	SF INC 1	Frames Counter No. 1 increment pulse.
A5J3	B1	GRD	
A5J3	A4	SF RS 1	Frames Counter No. 1 reset pulse.
A5J3	B3	GRD	
A5J3	A6	SF INC 2	Frames Counter No. 2 increment pulse.
A5J3	B5	GRD	
A5J3	A8	SFRS 2	Frames Counter No. 2 reset pulse.
A5J3	B7	GRD	
A5J3	A10	Spare	
A5J3	B9	Spare	
A5J3	A12	Spare	
A5J3	B11	Spare	
A5J3	D13	Spare	
A5J3	B13	Spare	
A5J3	C2	Spare	
A5J3	D1	Spare	
A5J3	C4	Spare	
A5J3	D3	Spare	
A5J3	C6	Spare	
A5J3	D5	Spare	
A5J3	C8	Spare	
A5J3	D7	Spare	
A5J3	C10	Spare	
A5J3	D9	Spare	
A5J3	C12	Spare	
A5J3	D11	Spare	
A5J3	E2	Spare	
A5J3	F1	Spare	

Table 3-5. Signal Identification for Rear Panel Connector A5J4 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J4	A2	PD01	Parallel data output bits 1 through 15.
A5J4	B1	GRD	
A5J4	A4	PD02	
A5J4	B3	GRD	
A5J4	A6	PD03	
A5J4	B5	GRD	
A5J4	A8	PD04	
A5J4	B7	GRD	
A5J4	A10	PD05	
A5J4	B9	GRD	
A5J4	A12	PD06	
A5J4	B11	GRD	
A5J4	D13	PD07	
A5J4	B13	GRD	
A5J4	C2	PD08	
A5J4	D1	GRD	
A5J4	C4	PD09	
A5J4	D3	GRD	
A5J4	C6	PD010	
A5J4	D5	GRD	
A5J4	C8	PD011	
A5J4	D7	GRD	
A5J4	C10	PD012	
A5J4	D9	GRD	
A5J4	C12	PD013	
A5J4	D11	GRD	
A5J4	E2	PD014	
A5J4	F1	GRD	
A5J4	E4	PD015	
A5J4	F3	GRD	

Table 3-5 (Cont'd.). Signal Identification for Rear Panel Connector A5J4 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J4	E6	PD016	Parallel data output bit 16.
A5J4	F5	GRD	
A5J4	E8	Spare	
A5J4	F7	Spare	
A5J4	E10	Spare	
A5J4	F9	Spare	
A5J4	E12	FRATE	Frame rate pulse.
A5J4	F11	GRD	
A5J4	H13	Spare	
A5J4	F13	Spare	
A5J4	G2	WDRATE	Word rate pulse.
A5J4	H1	GRD	
A5J4	G4	SF INC 1	Frame counter increment pulse.
A5J4	H3	GRD	
A5J4	G6	SF RS1	Frame counter reset pulse.
A5J4	H5	GRD	
A5J4	G8	Spare	
A5J4	H7	Spare	
A5J4	G10	Spare	
A5J4	H9	Spare	
A5J4	G12	Spare	
A5J4	H11	Spare	

Table 3-6. Signal Identification for Rear Panel Connector A5J5 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J5	A2	ADR1	
A5J5	B1	GRD	
A5J5	A4	ADR2	
A5J5	B3	GRD	
A5J5	A6	ADR3	
A5J5	B5	GRD	
A5J5	A8	ADR4	
A5J5	B7	GRD	
A5J5	A10	ADR5	
A5J5	B9	GRD	
A5J5	A12	ADR6	
A5J5	B11	GRD	
A5J5	D13	ADR7	Channel transfer lines 1 through 14.
A5J5	B13	GRD	
A5J5	C2	ADR8	
A5J5	D1	GRD	
A5J5	C4	ADR9	
A5J5	D3	GRD	
A5J5	C6	ADR10	
A5J5	D5	GRD	
A5J5	C8	ADR11	
A5J5	D7	GRD	
A5J5	C10	ADR12	
A5J5	D9	GRD	
A5J5	C12	ADR13	
A5J5	D11	GRD	
A5J5	E2	ADR14	
A5J5	F1	GRD	

Table 3-6 (Cont'd.). Signal Identification for Rear Panel Connector A5J5 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J5	E4	ADR15	Channel transfer lines 15 and 16.
A5J5	F3	GRD	
A5J5	E6	ADR16	
A5J5	F5	GRD	
A5J5	E8	DATA 1	Parallel data output bits 1 through 8.
A5J5	F7	GRD	
A5J5	E10	DATA 2	
A5J5	F9	GRD	
A5J5	E12	DATA 3	
A5J5	F11	GRD	
A5J5	H13	DATA 4	
A5J5	F13	GRD	
A5J5	G2	DATA 5	
A5J5	H1	GRD	
A5J5	G4	DATA 6	
A5J5	H3	GRD	
A5J5	G6	DATA 7	
A5J5	H5	GRD	
A5J5	G8	DATA 8	
A5J5	H7	GRD	
A5J5	G10	Spare	
A5J5	H9	Spare	
A5J5	G12	Spare	
A5J5	H11	Spare	

Table 3-7. Signal Identification for Rear Panel Connector A5J6 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J6	A2	ADR17	
A5J6	B1	GRD	
A5J6	A4	ADR18	
A5J6	B3	GRD	
A5J6	A6	ADR19	
A5J6	B5	GRD	
A5J6	A8	ADR20	
A5J6	B7	GRD	
A5J6	A10	ADR21	
A5J6	B9	GRD	
A5J6	A12	ADR22	
A5J6	B11	GRD	
A5J6	D13	ADR23	Channel transfer lines 17 through 30
A5J6	B13	GRD	
A5J6	C2	ADR24	
A5J6	D1	GRD	
A5J6	C4	ADR25	
A5J6	D3	GRD	
A5J6	C6	ADR26	
A5J6	D5	GRD	
A5J6	C8	ADR27	
A5J6	D7	GRD	
A5J6	C10	ADR28	
A5J6	D9	GRD	
A5J6	C12	ADR29	
A5J6	D11	GRD	
A5J6	E2	ADR30	
A5J6	F1	GRD	

Table 3-7 (Cont'd.). Signal Identification for Rear Panel Connector A5J6 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J6	E4	ADR31	Channel transfer lines 31 and 32.
A5J6	F3	GRD	
A5J6	E6	ADR32	
A5J6	F5	GRD	
A5J6	E8	DATA 9	Parallel data output bits 9 through 16.
A5J6	F7	GRD	
A5J6	E10	DATA 10	
A5J6	F9	GRD	
A5J6	E12	DATA 11	
A5J6	F11	GRD	
A5J6	H13	DATA 12	
A5J6	F13	GRD	
A5J6	G2	DATA 13	
A5J6	H1	GRD	
A5J6	G4	DATA 14	
A5J6	H3	GRD	
A5J6	G6	DATA 15	
A5J6	H5	GRD	
A5J6	G8	DATA 16	
A5J6	H7	GRD	
A5J6	G10	Spare	
A5J6	H9	Spare	
A5J6	G12	Spare	
A5J6	H11	Spare	

Table 3-8. Signal Identification for Rear Panel Connector A5J7 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J7	A2	ADR1	
A5J7	B1	GRD	
A5J7	A4	ADR2	
A5J7	B3	GRD	
A5J7	A6	ADR3	
A5J7	B5	GRD	
A5J7	A8	ADR4	
A5J7	B7	GRD	
A5J7	A10	ADR5	
A5J7	B9	GRD	
A5J7	A12	ADR6	
A5J7	B11	GRD	
A5J7	D13	ADR7	Channel transfer lines 1 through 14
A5J7	B13	GRD	
A5J7	C2	ADR8	
A5J7	D1	GRD	
A5J7	C4	ADR9	
A5J7	D3	GRD	
A5J7	C6	ADR10	
A5J7	D5	GRD	
A5J7	C8	ADR11	
A5J7	D7	GRD	
A5J7	C10	ADR12	
A5J7	D9	GRD	
A5J7	C12	ADR13	
A5J7	D11	GRD	
A5J7	E2	ADR14	
A5J7	F1	GRD	

Table 3-8 (Cont'd.). Signal Identification for Rear Panel Connector A5J7 (Ref. Figure 3-1)

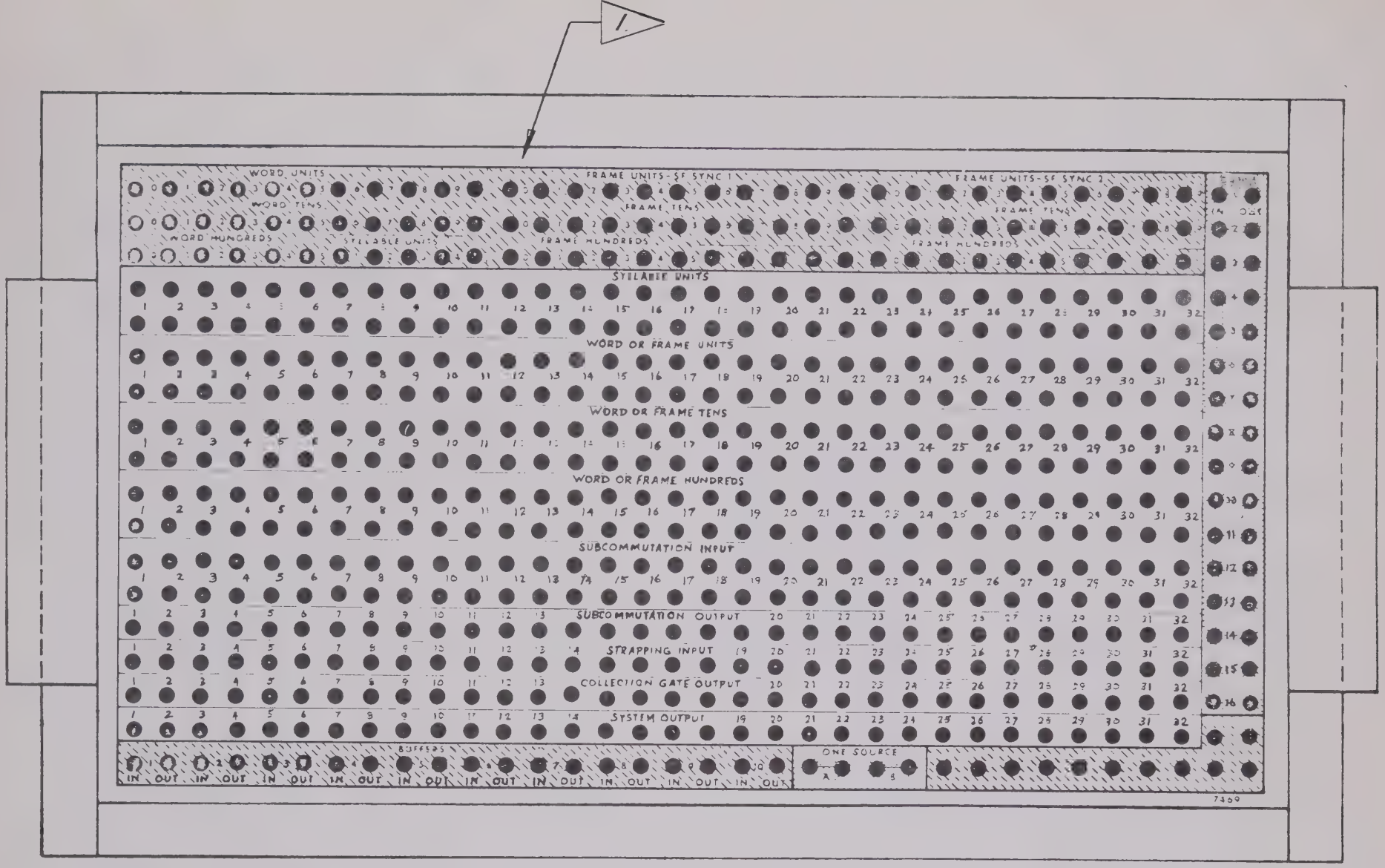
CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J7	E4	ADR15	Channel transfer lines 15 and 16.
A5J7	F3	GRD	
A5J7	E6	ADR16	
A5J7	F5	GRD	
A5J7	E8	DATA 1	Parallel data output bits 1 through 8.
A5J7	F7	GRD	
A5J7	E10	DATA 2	
A5J7	F9	GRD	
A5J7	E12	DATA 3	
A5J7	F11	GRD	
A5J7	H13	DATA 4	
A5J7	F13	GRD	
A5J7	G2	DATA 5	
A5J7	H1	GRD	
A5J7	G4	DATA 6	
A5J7	H3	GRD	
A5J7	G6	DATA 7	
A5J7	H5	GRD	
A5J7	G8	DATA 8	
A5J7	H7	GRD	
A5J7	G10	Spare	
A5J7	H9	Spare	
A5J7	G12	Spare	
A5J7	H11	Spare	

Table 3-9. Signal Identification for Rear Panel Connector A5J8 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J8	A2	ADR17	
A5J8	B1	GRD	
A5J8	A4	ADR18	
A5J8	B3	GRD	
A5J8	A6	ADR19	
A5J8	B5	GRD	
A5J8	A8	ADR20	
A5J8	B7	GRD	
A5J8	A10	ADR21	
A5J8	B9	GRD	
A5J8	A12	ADR22	
A5J8	B11	GRD	
A5J8	D13	ADR23	Channel transfer lines 17 through 30.
A5J8	B13	GRD	
A5J8	C2	ADR24	
A5J8	D1	GRD	
A5J8	C4	ADR25	
A5J8	D3	GRD	
A5J8	C6	ADR26	
A5J8	D5	GRD	
A5J8	C8	ADR27	
A5J8	D7	GRD	
A5J8	C10	ADR28	
A5J8	D9	GRD	
A5J8	C12	ADR29	
A5J8	D11	GRD	
A5J8	E2	ADR30	
A5J8	F1	GRD	

Table 3-9 (Cont'd.). Signal Identification for Rear Panel Connector A5J8 (Ref. Figure 3-1)

CONNECTOR	PIN	MNEMONIC	SIGNAL DESCRIPTION
A5J8	E4	ADR31	Channel transfer lines 31 through 32
A5J8	F3	GRD	
A5J8	E6	ADR32	
A5J8	F5	GRD	
A5J8	E8	DATA 9	Parallel data output bits 9 through 16
A5J8	F7	GRD	
A5J8	E10	DATA 10	
A5J8	F9	GRD	
A5J8	E12	DATA 11	
A5J8	F11	GRD	
A5J8	H13	DATA 12	
A5J8	F13	GRD	
A5J8	G2	DATA 13	
A5J8	H1	GRD	
A5J8	G4	DATA 14	
A5J8	H3	GRD	
A5J8	G6	DATA 15	
A5J8	H5	GRD	
A5J8	G8	DATA 16	
A5J8	H7	GRD	
A5J8	G10	Spare	
A5J8	H9	Spare	
A5J8	G12	Spare	
A5J8	H11	Spare	



NOTES:

1. SILK SCREEN BACKGROUND PER THE FOLLOWING:
   - MED CADMIUM YELLOW #BE-135
   - BRIGHT RED #BE-104
   - WHITE #BE-112
2. MADE FROM EMR DRAWING NO. 7469.

Figure 3-2. Patchboard Configuration

FROM PAGE 3-1

Each buffer is capable of driving 12 loads. The collection gate inputs and outputs are located in the central (yellow) area of the patchboard. The holes pertaining to a particular gate are located in one vertical column. Two jumpered patchboard holes are provided for all collection gate inputs (except the strapping inputs) in order that inputs or one-source signals can be applied to more than one gate.

The STRAPPING INPUTS patchboard area provides the capability of strapping a maximum of any 32 data channels in a format by outputting the channel transfer pulses on a common output line instead of on separate output lines.

The bottom row of the patchboard provides connection to the inputs and outputs of the ten buffers and also provides connection to the outputs of two one-source generators. Each one-source generator can be used to tie off up to 36 unused collection gate inputs.

The last two vertical columns on the patchboard are the DATA IN and DATA OUT columns. The parallel data multiplex from an external source is routed through the front panel INPUT switch to the DATA IN column on the patchboard. By appropriate patching to the DATA OUT column, the parallel data may be routed to external equipment in any bit order desired (MSB first, LSB first, etc.).

Certain areas of the patchboard are unused. The patchboard coordinates for each of the holes in these unused areas are as follows: L1, L2, L3, T3, U3, V3, W3, X1, X2, X3, AA18, BB18, CC18, DD18, EE3, EE18, FF3, FF18, GG3, GG18, HH3, HH18, JJ17, JJ18, KK17 and KK18. (See Figure 4-11 for coordinate locations.)

The SYSTEM OUTPUT row on the patchboard provides connections for routing the channel transfer pulses to external equipment via output connectors at the rear of the data distributor. Desired channel transfer pulses are patched from the COLLECTION GATE OUTPUT row to the SYSTEM OUTPUT row.

3.2.2 Patching Procedures

The patchboard provides the following programming capabilities:

a. Decommutation of syllables and words in every frame of incoming data.

b. Decommutation of syllables and words in selected frames of incoming data.

c. Strapping a maximum of any 32 data channels of incoming data, by outputting channel transfer pulses on a common output line.

d. Rearrangement of parallel data bit sequence on data distributor output lines.

Patching procedures for each of the programming capabilities listed are furnished in the following paragraphs.

3.2.2.1 Decommutation of Syllables or Words in Every Data Frame

To decommutate syllables or words in every frame of incoming data, proceed as follows:

a. If syllables are to be decommutated, patch syllable number from red SYLLABLE UNITS area to desired collection gate input in yellow SYLLABLE UNITS area.

b. Patch each word number from red WORD UNITS, WORD TENS, WORD HUNDREDS area to collection gate inputs in yellow WORD OR FRAME UNITS, WORD OR FRAME TENS, WORD OR FRAME HUNDREDS.

c. Tie off unused collection gate inputs by patching from ONE SOURCE A or B area to the collection gate input area and strapping all unused positions in that area.

d. The output of each counter stage is capable of driving 11 loads. If more driving capability is required, the BUFFERS area at the bottom of the patchboard must be used. Each of the 10 buffers is capable of driving 12 loads. For example, assume that words 200 through 231 of each frame of data are to be decommutated. In this case, the 2 hundreds stage of the Word Counter is used in each selection. Patching for the hundreds stage would be as follows:

(1) Patch from WORD HUNDREDS 2 area to collection gate 1 input in WORD OR FRAME HUNDREDS area.

(2) Strap collection gate inputs 1 through 10 in WORD OR FRAME HUNDREDS area.

(3) Patch from collection gate input 10 in WORD OR FRAME HUNDREDS area to BUFFERS 1 IN at bottom of patchboard.

(4) Patch from BUFFERS 1 OUT area at bottom of patchboard to collection gate input 11 in WORD OR FRAME HUNDREDS area.

(5) Strap collection gate inputs 11 through 21 in WORD OR FRAME HUNDREDS area.

(6) Patch from collection gate input 21 in WORD OR FRAME HUNDREDS area to BUFFERS 2 IN at bottom of patchboard.

(7) Patch from BUFFERS 2 OUT area at bottom of patchboard to collection gate input 22 in WORD OR FRAME HUNDREDS area.

(8) Strap collection gate inputs 22 through 32.

e. Patch from each COLLECTION GATE OUTPUT to a corresponding SYSTEM OUTPUT.

f. The parallel data input from the selected external source is routed through the front panel INPUT switch is routed to the DATA IN patch positions on the patchboard. If no data transposition is required, patch DATA IN 1 to DATA OUT 1, DATA IN 2 to DATA OUT 2, etc., for as many bits as there are in the syllables (or words). If data transposition is required; for example, MSB in to LSB out, or LSB in to MSB out, patch DATA IN 1 to DATA OUT N, DATA IN 2 to DATA OUT N-1, etc., where N equals the number of data bits per syllable (or word).

3.2.2.2 Decommutation of Syllables (or Words) in Selected Frames of a Subframe

To decommutate syllables or words of frames within a subframe, proceed as follows:

a. Perform steps a and b of paragraph 3.2.2.1.

b. Patch frame number from Frame Counter outputs (FRAME UNITS, FRAME TENS, FRAME HUNDREDS) to corresponding inputs on a collection gate.

c. Patch from the SUBCOMMUTATION OUTPUT of the collection gate selected in step b to the SUBCOMMUTATION INPUT of the collection gate selected in step a.

d. Patch from the COLLECTION GATE OUTPUT to the SYSTEM OUTPUT.

e. Repeat steps a through d for each subframe word selected.

f. Tie off unused collection gate inputs as described in paragraph 3.2.2.1.

g. Use BUFFERS area at bottom of patchboard as required.

h. Patch parallel data as described in 3.2.2.1.

Using the above procedures, a maximum of 16 channel transfer pulses may be generated, therefore a maximum of 16 subframe words may be selected from each incoming subframe. If the outputs of Frame Counter No. 2 (SF SYNC 2) are used, a maximum of 16 channel transfers may be generated; therefore a maximum of 16 subframe words may be selected using any combination of frame number outputs from Frame Counters No. 1 and No. 2 Figure 3-3 illustrates the patching for selecting a subframe word located in syllable 3 of word 357 in frame 349, with the channel transfer output on line 9. The DATA lines would be patched according to the number of bits in the syllable.

3.2.2.3 Strapping of Collection Gate Outputs

Provision is made for strapping a maximum of 32 data channels, by outputting the channel transfer pulses on a single output line instead of separate lines. The patching procedure for outputting 32 channel transfer pulses on a single output line is as follows:

a. Patch from COLLECTION GATE OUTPUT 1 through 31 to STRAPPING INPUT 2 through 32, respectively.

b. Strap from COLLECTION GATE OUTPUT 32 to desired SYSTEM OUTPUT line.

Strapping of smaller groups of data channels may be accomplished in a similar manner.

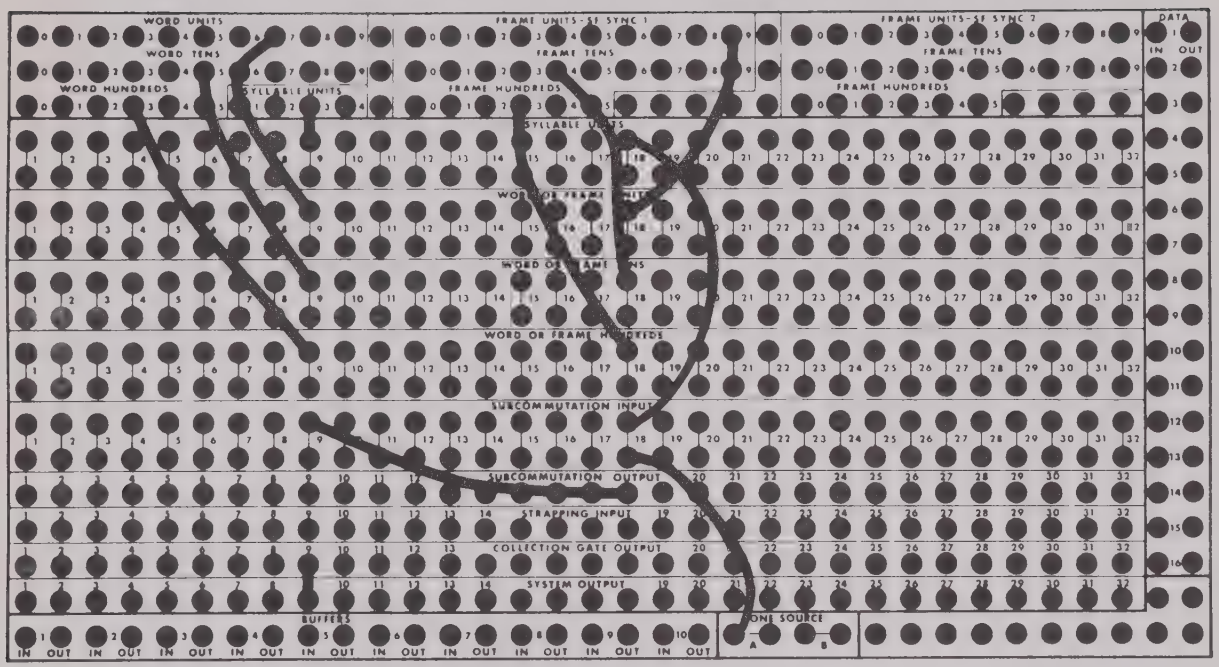
3.3 OPERATION

3.3.1 Controls and Indicators

The front panel controls and indicators for the data distributor are illustrated in Figure 3-4 and described in Table 3-10.

3.3.2 Preliminary Operating Procedures

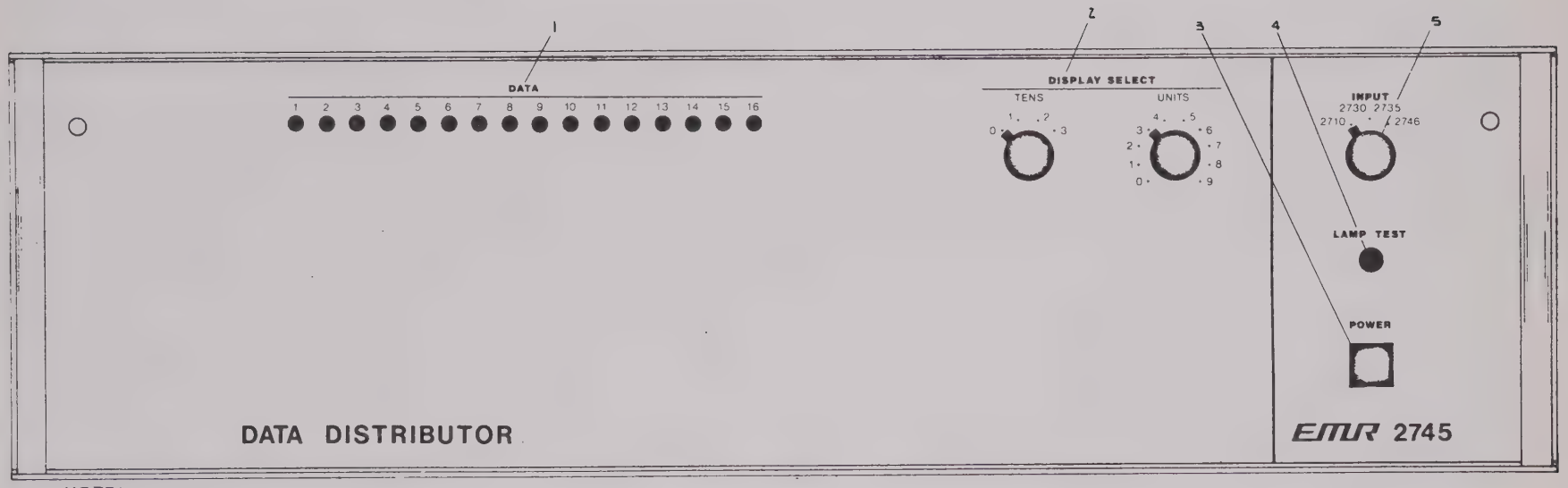
Before operating the unit, make all necessary external connections to the unit in accordance with particular system requirements. All external connections to the data distributor are made through connectors at the rear of the unit. The locations of these connectors are shown in Figure 3-1 and pin functions for connectors on connector assembly A5 are provided in Tables 3-2 through 3-9.



Note:

1. EMR Control No. 2745-004, Rev. A

Figure 3-3. Sample Patching Arrangement



NOTE:
1. MADE FROM EMR DWG. NO. 11171.

Figure 3-4. Location of Front Panel Controls and Indicators (Ref. Table 3-10)

Table 3-10. Function of Front-Panel Control and Indicators
(Ref. Figure 3-4)

REF. NO.	NAME	DESIG-NATION	FUNCTION
1	DATA 1 through DATA 16 display	A4A1DS1 through A4A1DS16	Display bit content of data word selected by DISPLAY SELECT switches.
2	DISPLAY SELECT UNITS and TENS rotary switches.	A4S3 and A4S2, respectively	Switches used for selecting any one of 32 collection gate outputs (channel transfer pulses) so that the bit content of the corresponding data word can be displayed at the DATA indicators.
3	POWER lighted pushbutton switch	A4S5	When depressed, connects AC input to Model 2650 Power Supply. The indicator lights when DC power is applied to the Model 2745.
4	LAMP TEST lighted push-button switch	A4S4	When depressed, lights all DATA indicators.
5	INPUT rotary switch	A4S1	Selects input source for data distributor. NOTE Position marked 2730/2735 also applicable for Model 2731 or 2736.

3.3.3 Operating Procedures

Operating procedures for the data distributor are as follows:

a. Remove patchboard from patchboard receiver and perform patching procedures in accordance with paragraph 3.2.

b. Insert programmed patchboard into receiver.

c. Depress POWER pushbutton switch and note that push-button indicator lights.

d. Depress LAMP TEST pushbutton switch and note that DATA 1 through DATA 16 indicators light while switch is depressed.

e. At DISPLAY SELECT switches, select channel number of data word to be displayed on DATA display lamps.

f. Set INPUT switch to proper input source.

SECTION 4

THEORY OF OPERATION

4.1 GENERAL

This section contains the data distributor theory of operation discussed at the detailed block diagram and logic levels. Figure 4-1 is the detailed block diagram of the unit. Each functional block in this figure contains a figure reference number which is the detailed logic diagram for that functional block. Diagrams for interface timing between the data distributor and external input sources (Models 2710, 2730/2731, 2735/2736, and 2746) are given in Figures 4-2 through 4-5. Input/Output timing relationships are illustrated in Figure 4-6. The file layout drawing, the detailed logic diagrams, the front panel switch schematic and the power distribution schematic are contained in Figures 4-7 through 4-14. A description of the symbology (mnemonics) and use of the logic diagrams is furnished in paragraph 4.3. Complete information on the digital logic cards used in the data distributor is furnished in Section 7 of this manual.

NOTE

All references in this section to the Model 2730 PCM Frame Synchronizer are also applicable to the Model 2731 PCM Frame Synchronizer. All references to the Model 2735 PCM Subframe Synchronizer apply to the Model 2736 PCM Subframe Synchronizer.

4.2 DETAILED THEORY OF OPERATION

4.2.1 Input Switching

As shown in Figures 4-1 and 4-8, front panel INPUT switch A4S1 permits selection of data and timing inputs from the Model 2710 PAM/PDM Signal Conditioner, the Model 2730 Frame Synchronizer, and the Model 2735 Subframe Synchronizer, or the Model 2746 PCM Decommutator. The INPUT switch is a three-position, 24-pole switch. Switch poles S1A1 through S1A4, S1B1 through S1B4, S1C1 through S1C4, and S1D1 through S1D4 route the parallel data inputs PDIN1 through PDIN16, directly to the patchboard. When the Model 2710 PAM/PDM Signal Conditioner is the input source, only 12 parallel data bits are routed as inputs to the data distributor. The remaining four input lines are tied to ground by switch poles S1D1 through S1D4 when the INPUT switch is set to the 2710 position.

The timing inputs to the data distributor are routed through INPUT switch poles S1E1 through S1E4 and S1F1 through S1F4. The frame rate (FRATE) pulse from a selected input source is routed through switch pole S1E1 as the word counter reset (WDRST) input to the Word Counter. Depending upon the setting of the INPUT switch, switch pole S1E2 receives a word rate (WDRATE) pulse from either the Model 2730 or 2746; or receives an output data request (OUTDRQ)

signal from the Model 2710. This signal is labeled word transfer (WDXFER) and is routed to the clock input of the Word Counter. When the Model 2730 is selected as the input source, the WDXFER pulse is also used as a preset (SYPRS) signal to the Syllable Counter. This signal is routed from the Word Counter through switch pole S1F3 to the Syllable Counter. Switch poles S1E3 and S1E4 receive the subframe counter no. 1 reset (SFRS1) and increment (SFINC1) pulses from either the Model 2735 or Model 2746. These signals are routed to Frame Counter No. 1 as reset (FR1RST) and clock (FR1CLK) inputs, respectively. Switch pole S1F1 routes the syllable rate (SYRATE) pulse from the Model 2730 to the Syllable Counter as an increment (SYXFER) input. When the INPUT switch is set to 2710 or 2746, switch pole S1F2 routes the word clock (WDCLK) developed in the Word Counter as a START command to the Strobe Generator. This input generates the strobe signal required for each data transfer output from the data distributor. When the INPUT switch is set to 2730/2735 switch pole S1F2 routes the syllables clock (SYCLK) developed in the Syllable Counter as the START command to the Strobe Generator. When the INPUT switch is set to 2730/2735, switch pole S1F4 routes a constant logic ONE level as an enable (FR2EN) input to Frame Counter No. 2. This signal conditions input gates in Frame Counter No. 2 so that clock (SFINC2) and resets (SFRS2) inputs from the Model 2735 Subframe Synchronizer can be routed to the counter clock and reset inputs. The SFINC2 and SFRS2 inputs are routed directly from the input connector to the input gates of Frame Counter No. 2.

4.2.2 Data Distributor Format Counters

The data distributro contains four format counters: the Syllable Counter, the Word Counter, Frame Counter No. 1 and Frame Counter No. 2. These counters are controlled entirely by timing inputs from the external source selected by data distributor INPUT switch A4S1. Each counter is described in conjunction with the detailed block diagram and the detailed logic diagram. Figures 4-2 through 4-5 illustrate the interface timing between the data distributor and the selected input source, and Figure 4-6 illustrates the timing relationship between data distributor inputs and outputs.

4.2.2.1 Syllable Counter

The syllable counter (Figures 4-1 and 4-9) is a four-stage unitary counter which is initially preset to a count of one by the SYPRS signal from the Input Switching. If either the Model 2710 or the Model 2746 is selected as the input source, SYPRS is a constant logic ONE and the Syllable Counter is held to a unitary count of one. If the Model 2730 is selected as an input source, SYPRS is the WDRATE input from the Model 2730 and every WDRATE pulse presets the Syllable Counter to a count of one.

The clock (SYCLK) input to Syllable Counter is 40 ns pulse derived from SYXFER which is a constant logic ONE if either the Model 2710 or the Model 2746 is selected as an input source. When the Model 2730 is selected as an input source, the SYXFER is the syllable rate (SYRATE) input from the Model 2730. The SYXFER pulse is shortened to a 40 ns SYCLK by a fixed one shot in the Syllable Counter logic because both WDRATE and SYRATE occur simultaneously when any word is

presented at the output of the Model 2730. With the SYRATE shortened into SYCLK, the first SYCLK is overridden by the SYPRS signal which presets the Syllable Counter to a count of one. The next SYCLK pulse advances the Syllable Counter to a count of two, etc. The four Syllable Counter outputs (SYL1 through SYL4) are routed to the patchboard for patching to the data distributor collection gates.

4.2.2.2 Word Counter

The Word Counter (Figures 4-1 and 4-10) consists of three unitary-type ring counters (units, tens and hundreds). The counters are wired so that the ninth stage of the units counter provides a carry to the tens counter and the ninth stage of the tens counter provides a carry to the hundreds counter. As previously discussed in paragraph 4.2.1, the Word Counter clock is a 72 ns pulse derived from the WDXFER signals and the Word Counter reset (WDRST) pulse is derived from the frame rate (FRATE) pulse supplied by the selected input source.

As shown in Figure 4-10, the units counter consists of 8-bit shift register J24X1 and JK flip-flops J24X2 and J24X3. In the reset condition, the units zero stage (WDU0) is a logic ONE and all other units stages are logic ZERO's. The first clock pulse sets the units one stage (WDU1) to a logic ONE and all other stages to logic ZERO's. This process continues until the ninth clock pulse sets WDU9 to a logic ONE and all other stages to logic ZERO's. The tenth clock pulse causes the logic ONE in the ninth stage to be fed back to the zero stage (WDU0) and all other stages become logic ZERO's. In addition, when WDU9 is logic ONE, gate J22X1 enables the next clock pulse (WDCLK) to be fed into the tens counter (J25X1, J25X2, and J25X3). This same type gating through J22X2 allows a clock pulse to enter the hundreds counter (J26X1 and J26X2) when both the units ninth stage and the tens ninth stage are ones.

At the end of a frame of data, zero stages (WDU0, WDT0 and WDH0) of the units, tens and hundreds counters are reset to logic ONE's and all other stages of the units, tens and hundreds counters are reset to logic ZERO's by the WDRST pulse.

All Word Counter outputs (units 0-9, tens 0-9 and hundreds 0-5) are routed to the corresponding WORD UNITS, WORD TENS and WORD HUNDREDS area of the patchboard for patching to the data distributor collection gate inputs.

4.2.2.3 Frame Counters No. 1 and No. 2

Frame Counter No. 1 (Figures 4-1 and 4-10) circuit operation is identical to that described for the Word Counter except that the pulse duration of the frame clock (FR1CLK) is utilized exactly as received from the Model 2735 or 2746.

Frame Counter No. 2 is used only when the Model 2735 is selected as the input source because the 2746 accommodates only one subframe synchronizer at a time. The clock (SFINC2) and reset (SFRS2) inputs to Frame Counter No. 2 are routed to input gates J22X7 and J22X8. These gates are enabled by a logic ONE level (FR2EN) only when the INPUT select switch is set to the 2730/2735 position.

The units, ten and hundreds outputs of Frame Counter No. 1 are routed to the corresponding FRAME UNITS, FRAME TENS and FRAME HUNDREDS positions in the SF SYNC 1 area of the patchboard for patching to the collection gate inputs. The units, tens and hundreds outputs of Frame Counter No. 2 are routed to the corresponding FRAME UNITS, FRAME TENS and FRAME HUNDREDS positions in the SF SYNC 2 area of the patchboard for patching to the collection gate inputs.

4.2.2.4 Format Counter Output Loading

The output of each counter stage is capable of driving 11 standard logic loads. Normally, each buffer-type flip-flop can drive 12 loads, but in the shift register configuration, each stage must drive the following stage in addition to the external loading. Inverters J27X5, X6 (Word Counter), X7, X8, (Frame Counter No. 1), X15, and X16 (Frame Counter No. 2), are provided in order that the units ninth stage and the tens ninth stage of each counter retains the 11-load driving capability. Additional load driving capability may be obtained by use of the ten Counter Fanout Buffers, whose inputs and outputs are connected to the BUFFERS area of the patchboard. Each buffer has the capability of driving 12 loads. Patching procedures for using these buffers are provided in paragraph 3.2.2 and patchboard shunts for collection gate inputs are shown in Figure 4-11.

4.2.3 Collection Gates

The Collection Gates (Figure 4-1 and Figure 4-12) consist of 32 independent gating circuits. Each gating circuit can receive patched inputs from the Syllable, Word and Frame Counters, subcommutation inputs patched from other collection gates, and the strapped outputs of other collection gates. A strobe input, connected to each of the 32 collection gate circuits, enables a channel transfer pulse output from any collection gate circuit when the proper patched count occurs.

As shown in Figure 4-12, each collection gate circuit consists of three gates. The eight-input gate serves as an AND-gate, collecting the various counter conditions. The two-input gate serves as an OR-gate, OR'ing the eight-input collection gate output and the output of any other patched gate in order to perform the strapping function. The OR-gate output may be routed back to the input of another collection gate via the SUBCOMMUTATION OUTPUT and SUBCOMMUTATION INPUT areas of the patchboard if subcommutation is used. The OR-gate output is also applied to a one-input gate which serves as an inverter. The inverter output (channel transfer pulse) is routed to a COLLECTION GATE OUTPUT at the patchboard.

4.2.3.1 Strobe Input to Collection Gates

A common STROBE input is routed to the 32 collection gate circuits. The STROBE signal is generated from the output data request (OUTDRQ) when the Model 2710 is the input source, from the SYRATE signal when the Model 2730 is the input source, or from the WDRATE signal when the Model 2746 is the input source. The resulting START input to the Strobe Generator is delayed approximately 403 ns before generating the STROBE output to ensure that all format counters and patched signals are stable. The STROBE signal enables a channel transfer pulse output

(approximately 259 ns in duration) from any of the 32 collection gate circuits when the proper patch count occurs.

4.2.3.2 Syllable Count Inputs to Collection Gates

The syllable count inputs (GnSYL) to the collection Gates are patched from either the 1, 2, 3, or 4 count output of the Syllable Counter. If syllabization is not used, the syllable count inputs are patched to either a one-source or to the SYL1 output of the Syllable Counter in order to eliminate the possibility of noise causing erroneous collection gate outputs.

4.2.3.3 Word or Frame Count Inputs to Collection Gates

The word or frame count inputs (GnU, GnT, and GnH) are patched from the units, tens, and hundreds outputs of the Word Counter or one of the Frame Counters. The following conditions govern this patching:

(a) Commutated Data - When subcommutation is not used, the Word Counter output is patched into the GnU, GnT and GnH positions for the respective collection gate.

(b) Subcommutated Data - When subcommutation is used, one collection gate is patched with the word count during which the respective data appears. Another collection gate is patched with the frame count during which the respective data appears. The subcommutation (GnSC) input of either of these collection gates is then patched from the subcommutation (GmSCO) output of the other gate. The unused GmSC input is tied off to a one-source and the GnOUT is patched to the respective system output. In cases where more than one frame collection gate is patched with respect to one main frame word, the word collection gate can drive (without buffering) up to five frame collection gates. In the same manner, if one frame count is to be patched with respect to more than one word count, the frame collection gate can drive up to five word collection gates.

4.2.3.4 Strapping Input to Collection Gates

The strapping inputs (GnSTP) are utilized when strapped words or frames are to be decommutated. The collection gate outputs (GnOUT) of strapped gates are patched into the strapping inputs (GnSTP) of the strapped gates. As an example, consider that three data words are to be strapped using collection gates 1, 2, and 3. The three word counts are patched into gates 1, 2, and 3, respectively. The G1OUT of Gate 1 is patched to the G2STP input of Gate 2, the G2OUT is patched to G3STP, and the G3OUT is the collection gate output which provides a channel transfer pulse when any of the three data words occur. G3OUT signal is then patched to the required system output.

4.2.3.5 Collection Gate Outputs

The output (GnOUT) of any collection gate can be patched to any one of the 32 system output positions. The system outputs are labeled on the patchboard with respect to the output connector wiring, for example: SYSTEM OUTPUT 1 is wired to Address Output 1 (ADR 1).

4.2.4 Data Handling

4.2.4.1 Data Output

As shown in Figures 4-1 and 4-8, the parallel data inputs (PDIN1 through PDIN16) from the selected source are routed from the INPUT select switch to 16 patchboard holes labeled DATA IN 1 through DATA IN 16. These signals can then be patched (in any sequence or bit alignment) to the 16 patchboard holes labeled DATA OUT 1 through DATA OUT 16. Each Data OUT signal (relabeled DOn) is wired from the patchboard through two inverters to the data output connectors. The output leads are labeled DATA 1 through DATA 16. (Figures 4-1 and 4-13)

4.2.4.2 Data Display

The $\overline{\text{DOn}}$ signals (Figures 4-1 and 4-13) are routed to the data input pins of four 4-bit storage registers. The reset (RSTDSP) and strobe (STODSP) signals to these registers are derived when a particular system output (collection gate) becomes active and that output is selected with the DISPLAY SELECT switch. When such a selection is made, and the DISPLAY SELECT switch common goes to zero level, the output from pin 40 of J33 goes to the one level, thus resetting the display storage registers (J13 and J14). When the DISPLAY SELECT switch goes back to the one level, the reset condition is deleted, and the output at pin 24 of J13 causes FOS J39X4 and GOS J39X7 to fire, and the data word is stored in the display storage registers.

4.2.5 Power Distribution

Power is supplied to the Model 2745 by the EMR Model 2650 Power Supply designated APS1. Figure 4-14 illustrates power supply terminal board APS1TB1 and POWER switch A4S5 which connects the AC input to the power supply. The DC outputs of the power supply are routed through APS1TB1 to the digital logic cards and display card A4A1. The display card schematic is shown in Figure 4-15. Detailed information on the Model 2650 Power Supply is provided in the instruction manual for that unit.

4.3 LOGIC DIAGRAMS

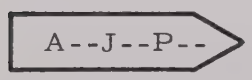
Five logic diagrams (Figures 4-8 through 4-10, 4-12 and 4-13) are included in this section. Figure 4-7, the Data Distributor File Layout, is the key diagram in the set. This figure illustrates the layout of the printed-circuit card file assembly A1. The file layout also provides the EMR model number or assembly number and the type of each printed-circuit card used in each plug-in socket. For example, assembly A1, location J26 (A1J26), contains the EMR Model 2567, One 8-to-10 Bit Shift Register B (1-8/10 SRB).

In the A1J26 column at circuit numbers 1 through 3, there are three numbered codes: 1-1, 1-1 and 3-1. The first digit of each code designates the Model 2745 logic function which uses this circuit. The second digit of each code is the logic diagram sheet number which contains the circuit. The table at the right side of Figure 4-7 lists each logic function by number and provides the figure number and number of sheets for each logic diagram which illustrates the function. Thus, the 1-8/10 SRB in A1J26 is used in Figures 4-9 and 4-10.

Conversely, see Figure 4-10, sheet 1. At the bottom center of the sheet, there is a rectangular block named "8 BIT SHIFT REGISTER B".. Above the upper right corner of the block appears the designation "J26X1". The "X1" indicates that this is circuit 1 on the printed-circuit card in location J26; note 3 at the lower left of the sheet indicates that this location is in Assembly A1.

A complete description of the EMR Model 2500 printed-circuit cards (and other special cards used in the Model 2745) is contained in Section 7. Thus, to determine the logical and electrical operation of any circuit illustrated in Figures 4-8 through 4-13), refer the code above the symbol (which contains assembly numbers, card location, and card circuit) to Figure 4-7 to determine the four-digit model or assembly number of the card. Then refer to the card description in Section 7.

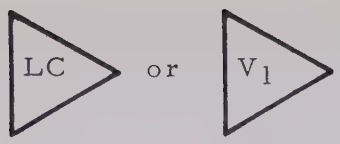
The function of three other symbols used in the logic diagrams is defined as follows:



Indicates the signal is to or from another circuit in the same function (usually in the same figure but a different sheet).

Indicates the signal is to or from another circuit in a different function (shown in a different figure).

Indicates a common connection within a circuit module. (For typical example, see a schematic for Model 2501 logic circuit in Section 7)



Indicates a binary ONE level voltage source.

Table 4-1 defines the abbreviated signal names (mnemonics) appearing throughout the logic diagrams.

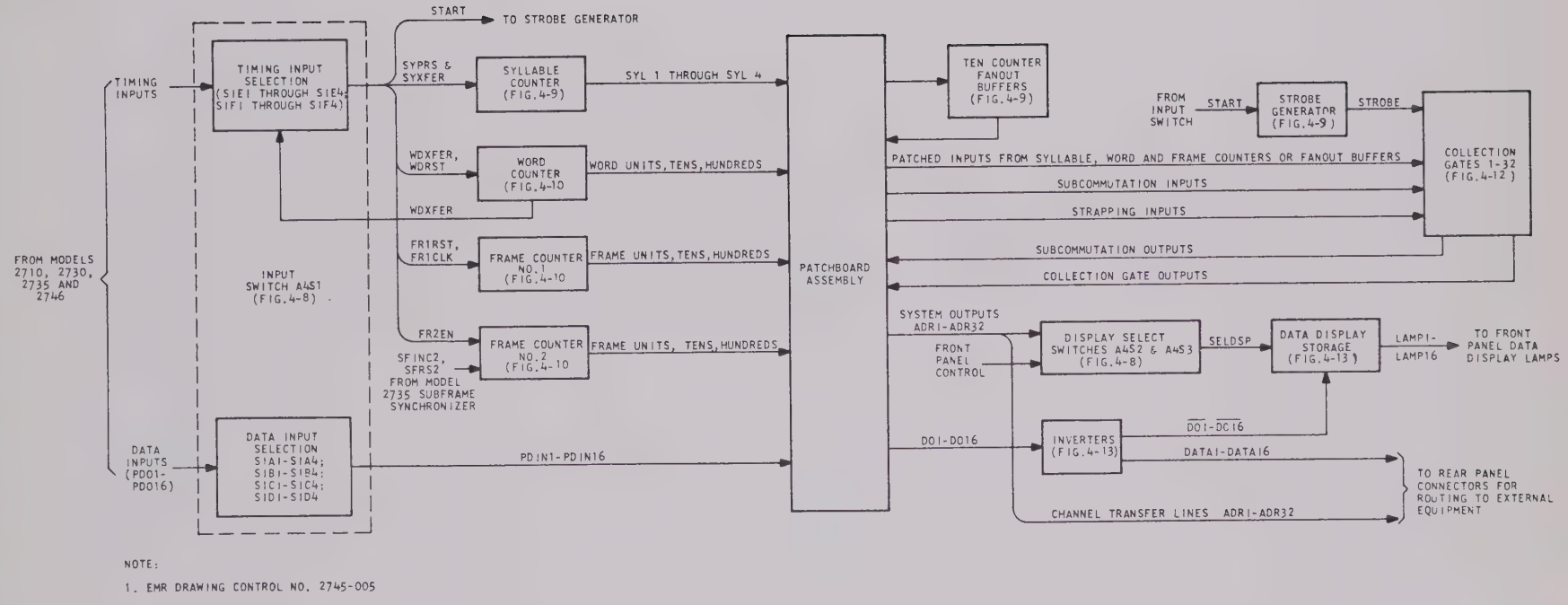
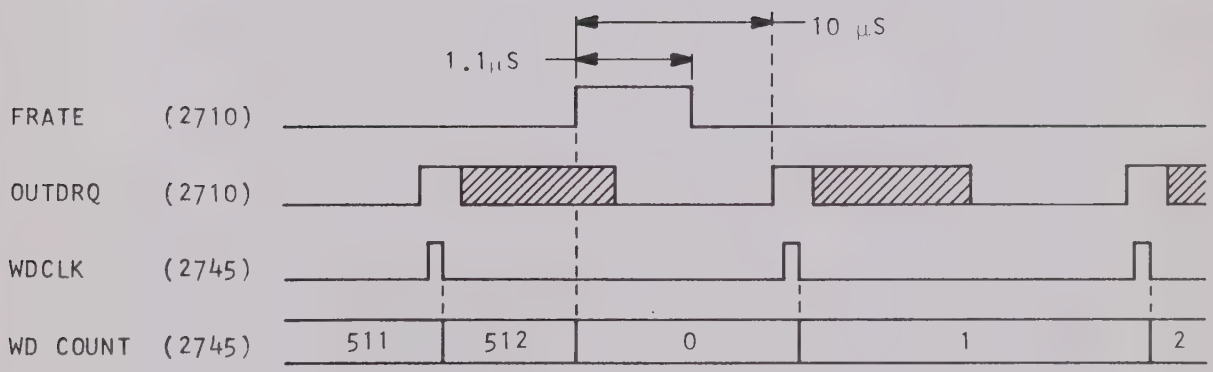
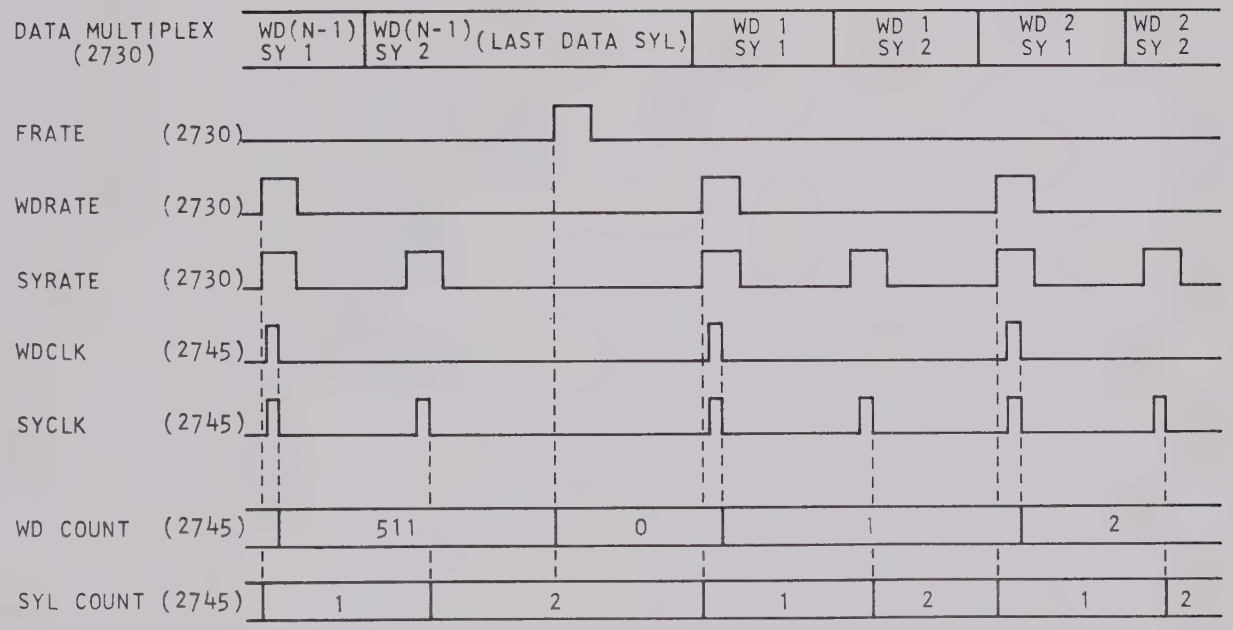


Figure 4-1. Model 2745 Detailed Block Diagram



NOTE:
1. EMR DRAWING CONTROL NO. 2745-006

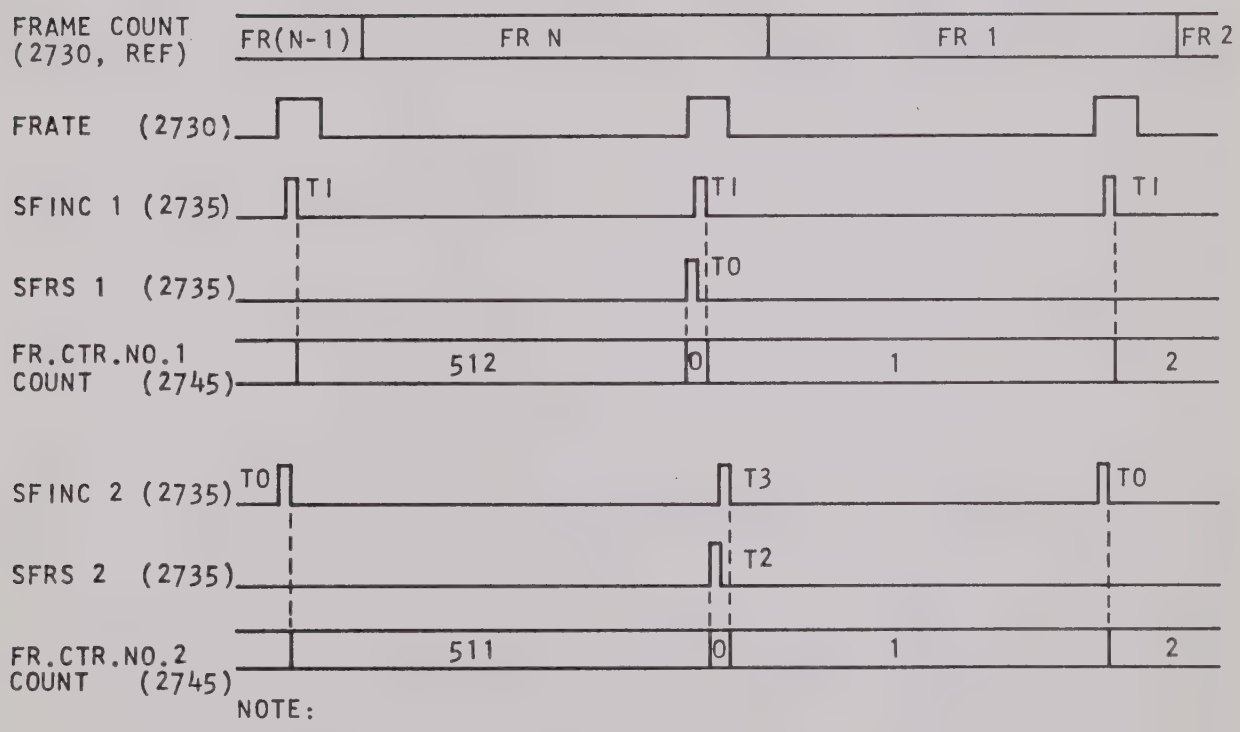
Figure 4-2. Interface Timing Diagram with Model 2710 as Input Source



NOTE:

1. EMR DRAWING CONTROL NO. 2745-007

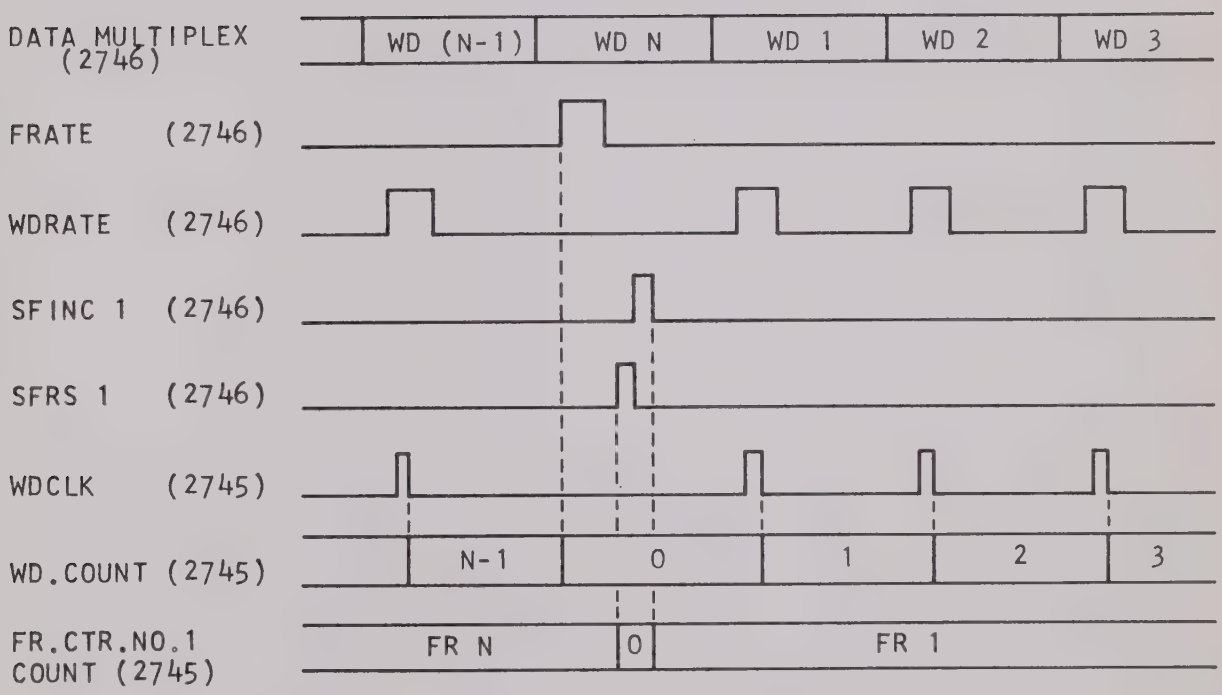
Figure 4-3. Interface Timing Diagram with Model 2730/2731 as Input Source



NOTE:

1. EMR DRAWING CONTROL NO. 2745-008

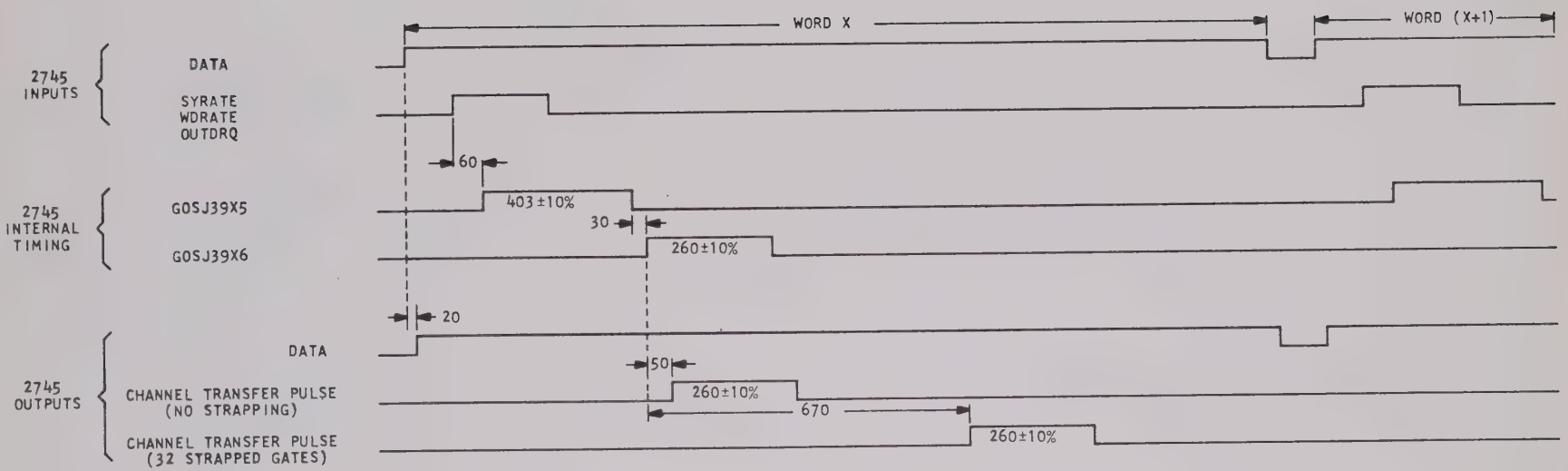
Figure 4-4. Interface Timing Diagram with Model 2735/2736 as Input Source



NOTE:

1. EMR DRAWING CONTROL NO. 2745-009

Figure 4-5. Interface Timing Diagram with Model 2746 as Input Source



NOTES:

1. ALL TIMES ARE IN NANOSECONDS.
2. TIMES GIVEN WITHOUT TOLERANCES ARE DERIVED FROM TYPICAL LOGIC GATE DELAY TIMES (1 DELAY≃10 NS).
3. EMR DRAWING CONTROL NO. 2745-010.

Figure 4-6. Model 2745 Input/Output Timing Diagram

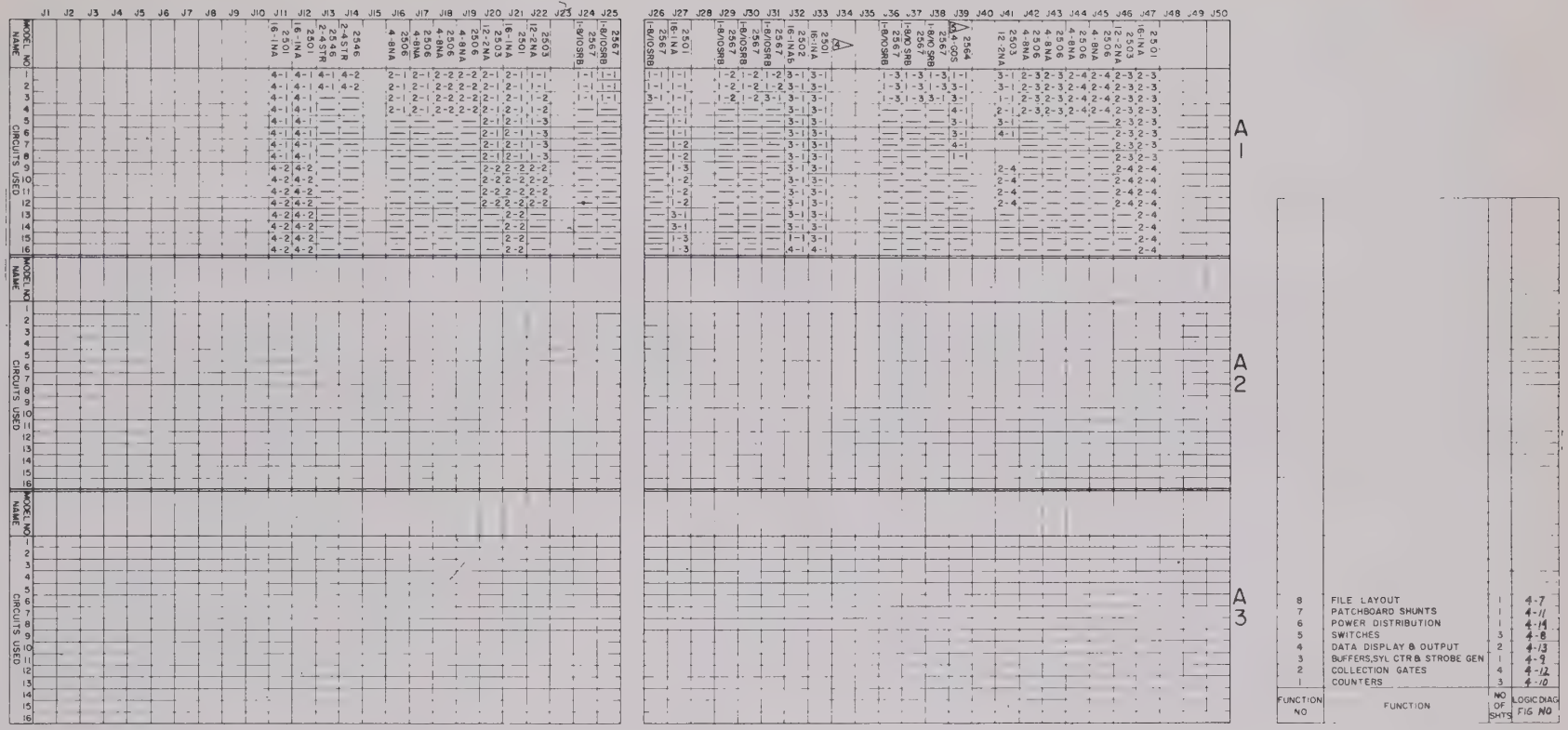
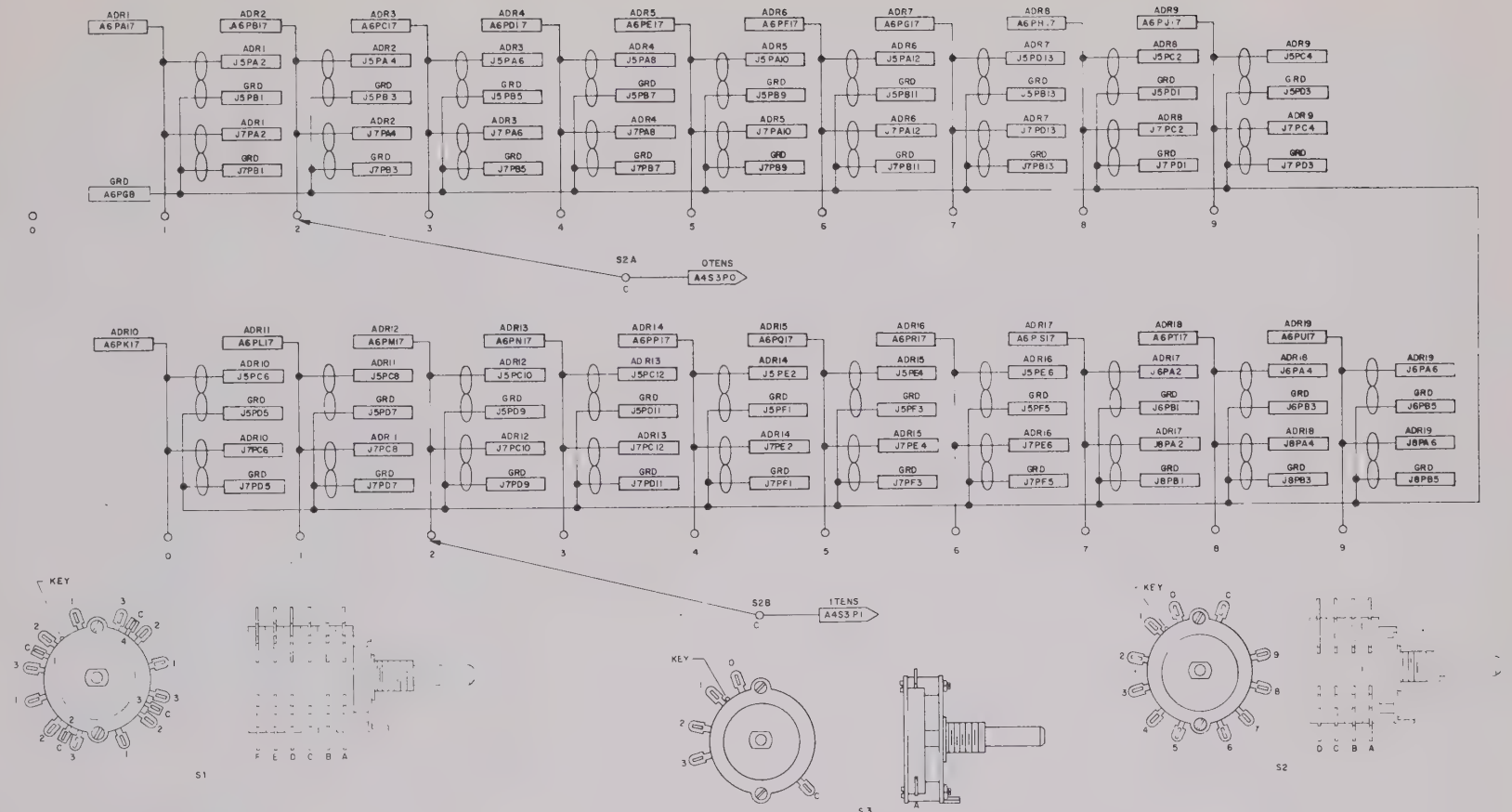

A1
A2
A3
NOTES
1 VERTICAL LINE THRU ALL CIRCUITS INDICATES UNUSABLE CARD SLOT
2 HORIZONTAL LINE IN CIRCUITS USED BLOCK INDICATES THAT CIRCUIT IS NOT ON THE CARD
3 NUMBER APPEARING IN CIRCUITS USED BLOCK ARE CODED THUS FUNCTION NO —— 9-4 —— SHEET NUMBER OF THE FUNCTION ON WHICH THIS CIRCUIT APPEARS.
4 RESISTOR CARD-ASSY NO 8301 CKTS 34 & 35 NOT USED
5 GOS: TIMING CAPACITORS ARE AS FOLLOWS:
CKT LOCATION | CAP | VALUE | PART NO. | CONNECTION
A1J39X5 | C9 | 56PF | 304-13-05609 | E1 E2
A1J39X6 | C10 | 36PF | 304-08-03609 | E3-E4
A1J39X7 | C11 | 36PF | 304-08-03609 | E5 E6
A1J39X8 | C12 | 10PF | 304-01-01009 | E7-E8
6. EMR DRAWING NO. 7476 - REV. 8
8 FILE LAYOUT 1 4-7
7 PATCHBOARD SHUNTS 1 4-11
6 POWER DISTRIBUTION 1 4-14
5 SWITCHES 3 4-8
4 DATA DISPLAY & OUTPUT 2 4-13
3 BUFFERS,SYL CTR & STROBE GEN 1 4-9
2 COLLECTION GATES 4 4-12
1 COUNTERS 3 4-10
FUNCTION NO
FUNCTION
NO OF SHTS
LOGIC DIAG FIG NO

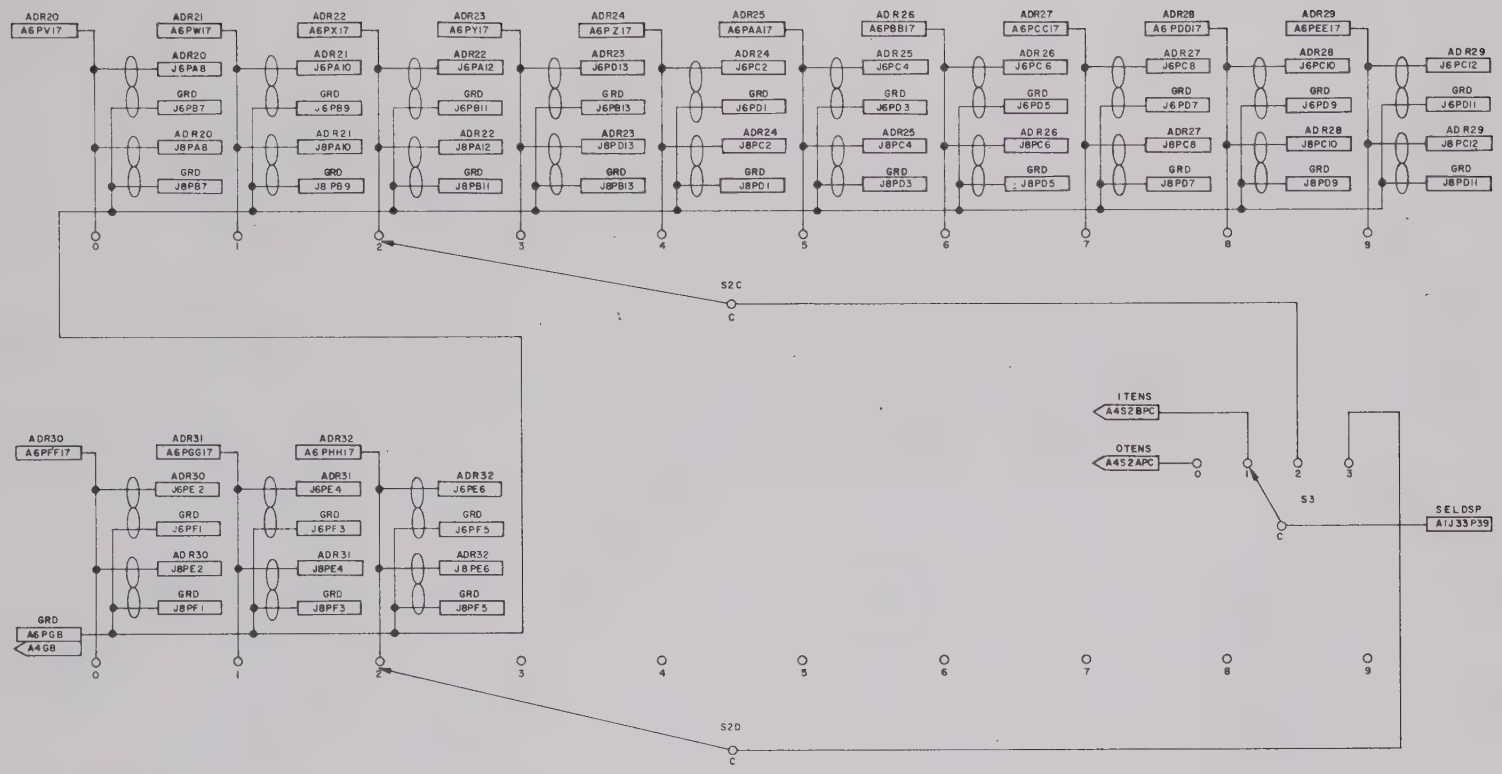
Figure 4-7 File Layout



5. EMR DRAWING NO. 7621 (SHEET 1 OF 3) - REF. 3
4. GROUND BUSS CONNECTED DURING MECHANICAL ASSEMBLY
3. S2 IS A 10 POSITION 4 POLE SWITCH APPEARING ON SHEETS 1 AND 2
2. ALL S NUMBERS ARE PREFIXED BY A4
1. ALL JACK AND PIN NUMBERS (J__P__) APPEARING IN RECTANGULAR FLAGS ARE PREFIXED BY A5 UNLESS OTHERWISE INDICATED

NOTES

Figure 4-8. Data Distributor Switches, Schematic Diagram (Sheet 1 of 3)



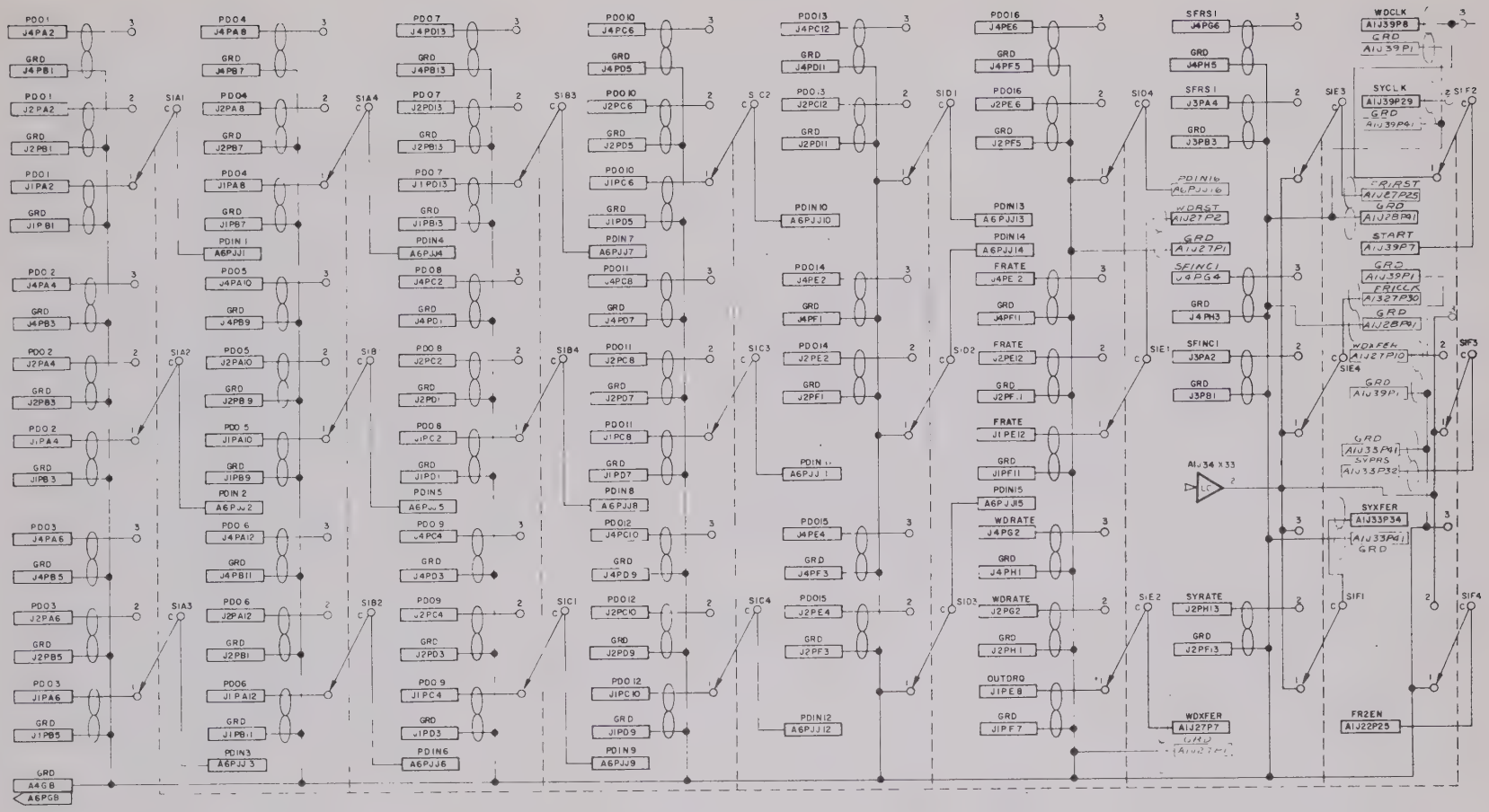
3 EMR DRAWING NO 7481 (SHEET 2 OF 3)

2 ALL S NUMBERS ARE PREFIXED BY A4

1. ALL JACK AND PIN NUMBERS APPEARING IN RECTANGULAR FLAGS ARE PREFIXED BY A5 UNLESS OTHERWISE INDICATED.

NOTES:

Figure 4-8. Data Distributor Switches, Schematic Diagram (Sheet 2 of 3)



2 ALL S NUMBERS ARE PREFIXED BY A4.

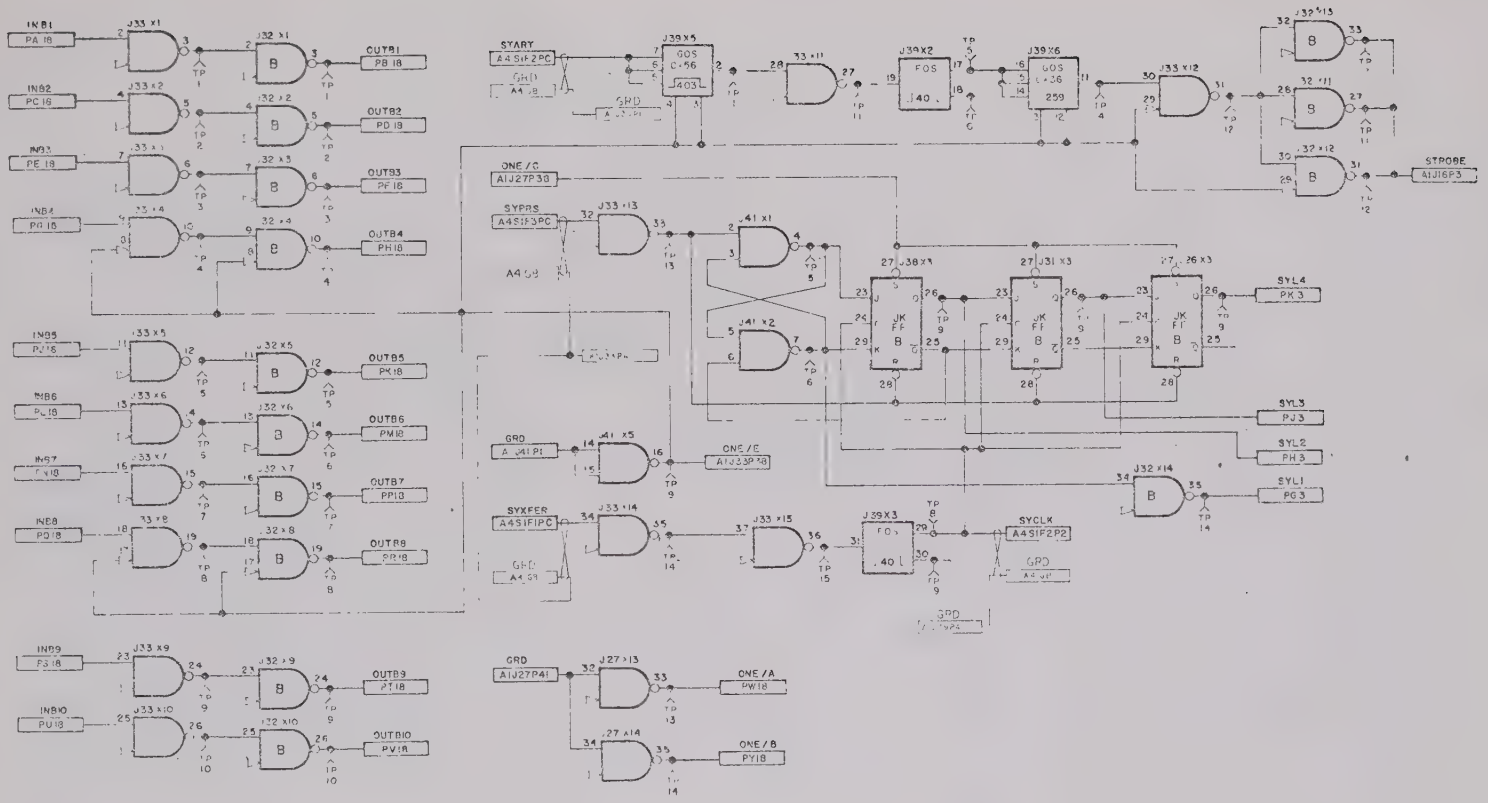
ALL JACK AND PIN NUMBERS [illegible] APPEARING IN FLAGS ARE PREFIXED BY A5 UNLESS OTHERWISE NOTED.

NOTES

3 SWITCH POSITION 1 SELECTS INPUTS FROM 2710
SWITCH POSITION 2 SELECTS INPUTS FROM 2730 & 2735
SWITCH POSITION 3 SELECTS INPUTS FROM 2746

(NOTES)

Figure 4-8. Data Distributor Switches, Schematic Diagram (Sheet 3 of 3)



4. THR DRAWING NO. 7479-REV. B
3. ONE SHOT: TIME EXPRESSED IN N SEC AND C IN PF UNLESS OTHERWISE INDICATED.
2. ALL PIN NUMBERS APPEARING IN RECTANGULAR FLAGS (P___) ARE PREFIXED BY A6 UNLESS OTHERWISE INDICATED.
1. ALL LOGIC SYMBOL JACK AND CIRCUIT NUMBERS (J__X__) ARE PREFIXED BY A1 UNLESS OTHERWISE INDICATED.

NOTES:

Figure 4-9. Buffers, Syllable Counter and Strobe Generator, Logic Diagram

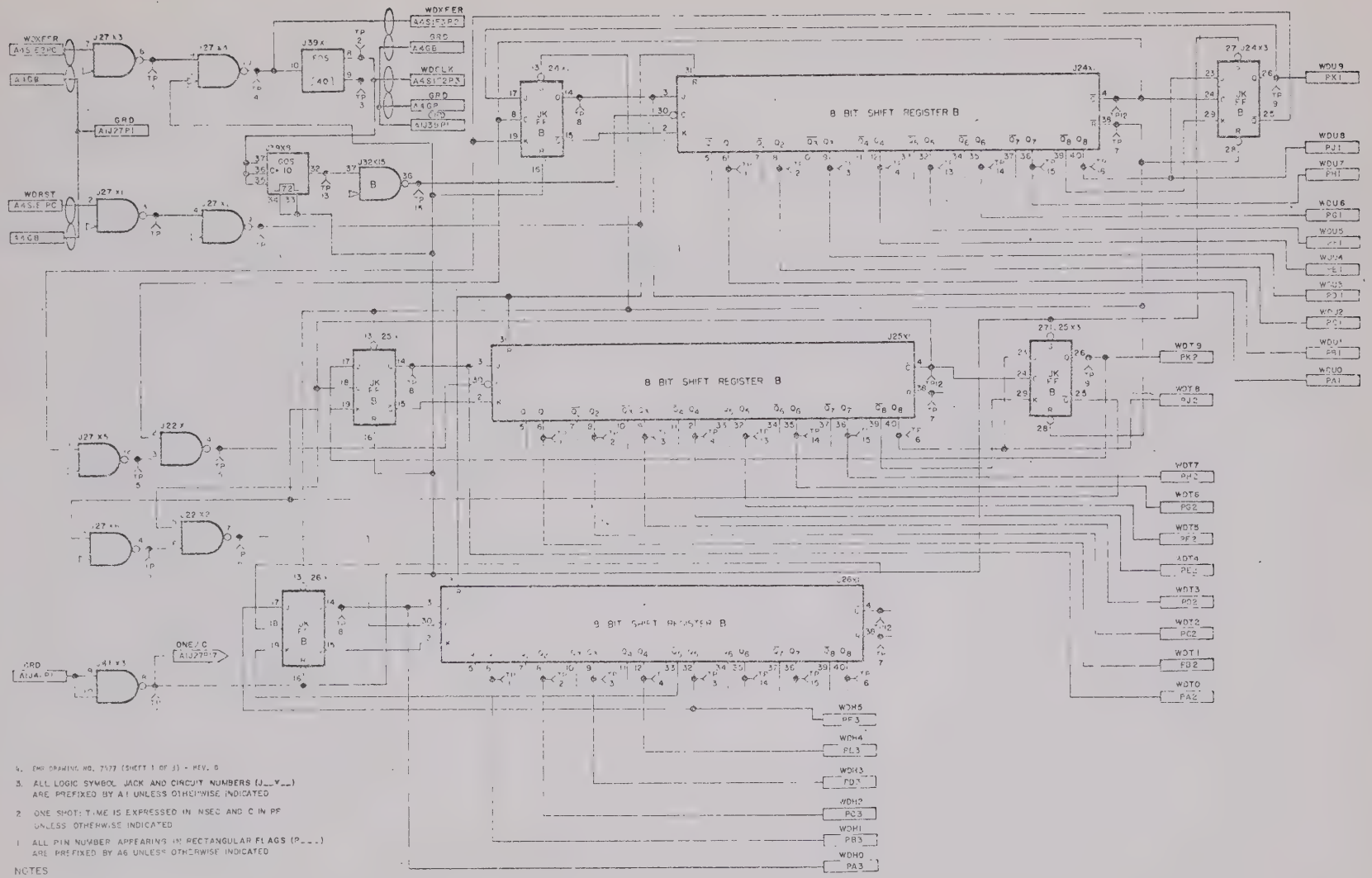


Figure 4-10. Word and Frame Counter, Logic Diagram (Sheet 1 of 3)

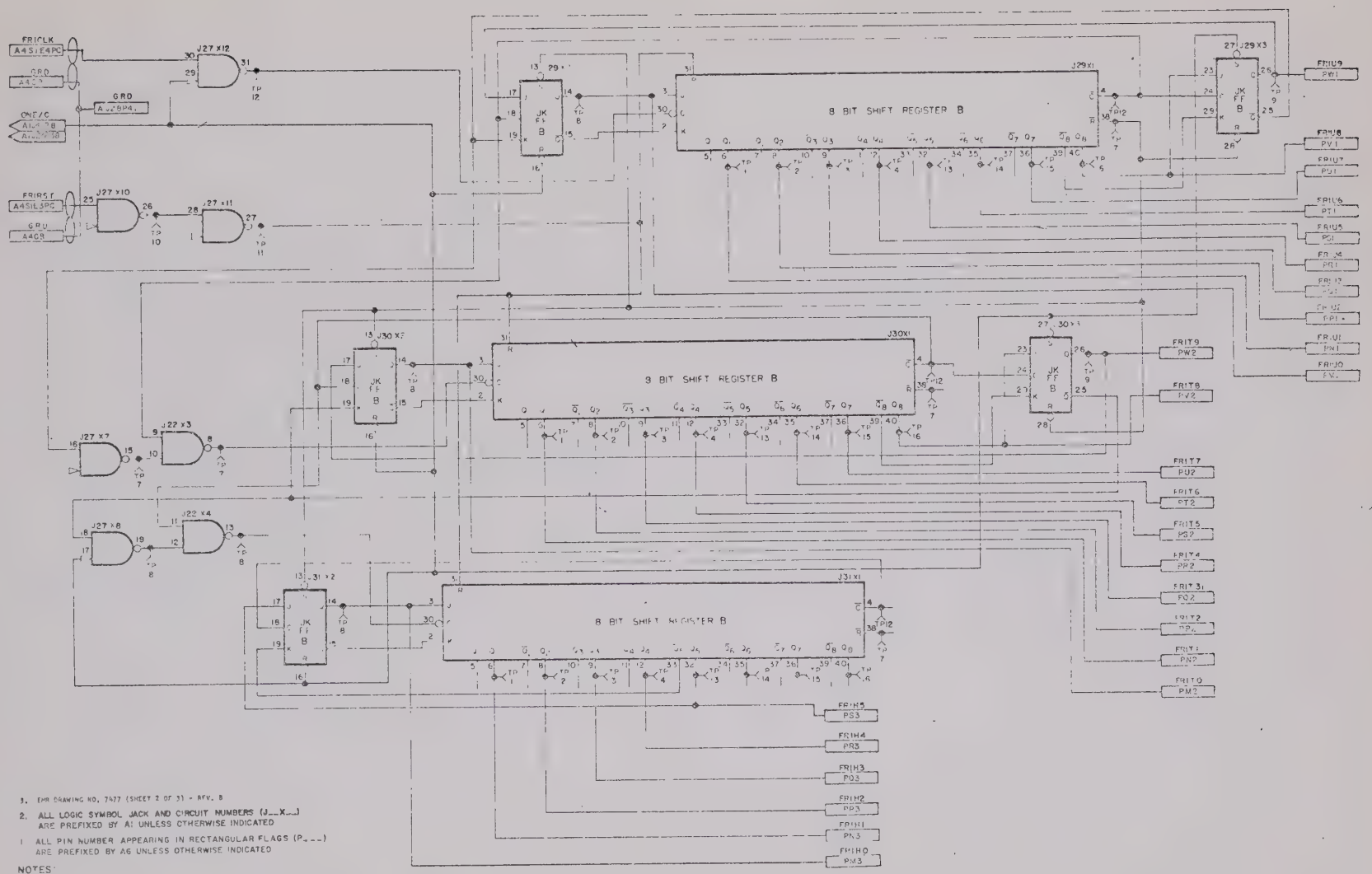

8 BIT SHIFT REGISTER B
8 BIT SHIFT REGISTER B
8 BIT SHIFT REGISTER B
JK FF B
NOTES:
1. ALL PIN NUMBER APPEARING IN RECTANGULAR FLAGS (P___) ARE PREFIXED BY A6 UNLESS OTHERWISE INDICATED
2. ALL LOGIC SYMBOL JACK AND CIRCUIT NUMBERS (J__X__) ARE PREFIXED BY A1 UNLESS OTHERWISE INDICATED
3. EMR DRAWING NO. 7477 (SHEET 2 OF 31) - REV. B

Figure 4-10. Word and Frame Counter, Logic Diagram (Sheet 2 of 3)

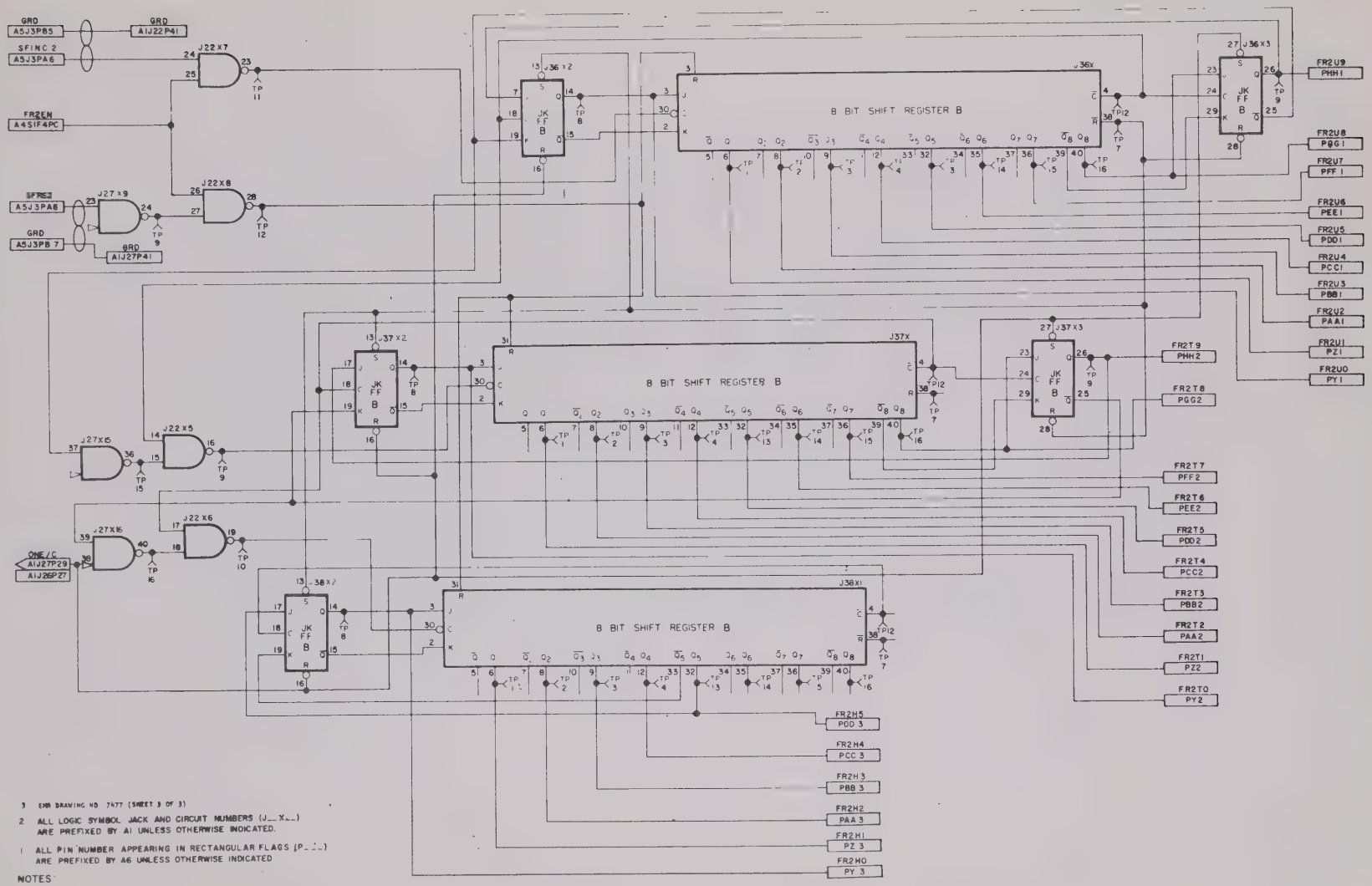


Figure 4-10. Word and Frame Counter, Logic Diagram (Sheet 3 of 3)

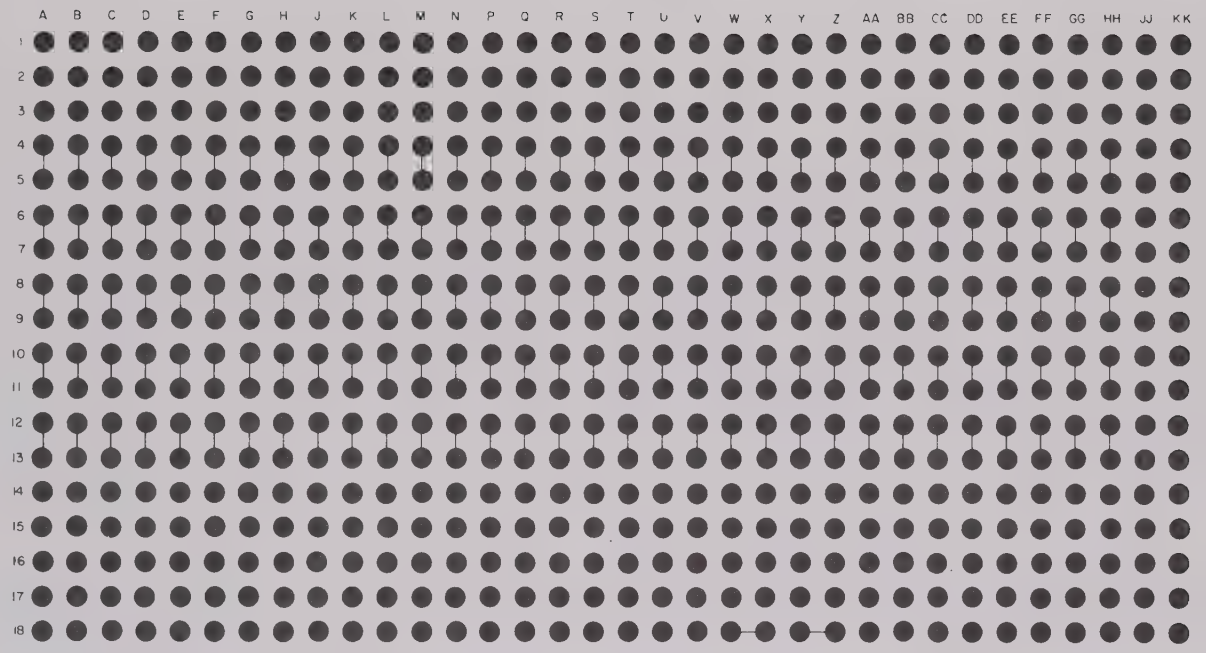
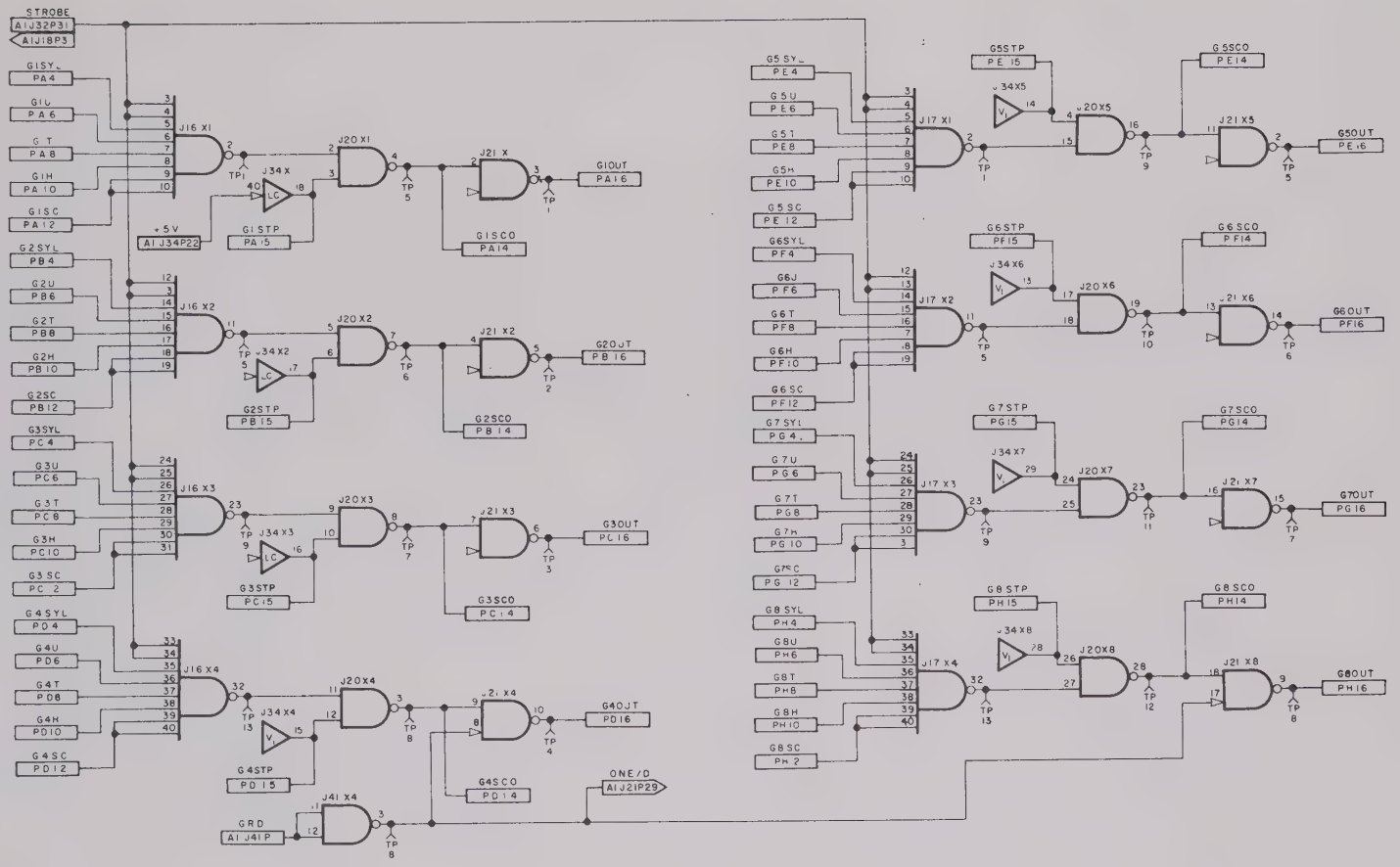

A B C D E F G H J K L M N P Q R S T U V W X Y Z AA BB CC DD EE FF GG HH JJ KK
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
NOTES:
1. LINES BETWEEN HOLES INDICATE WIRED CONNECTIONS BETWEEN RESPECTIVE PINS.
2. EMR DRAWING NO. 7483.

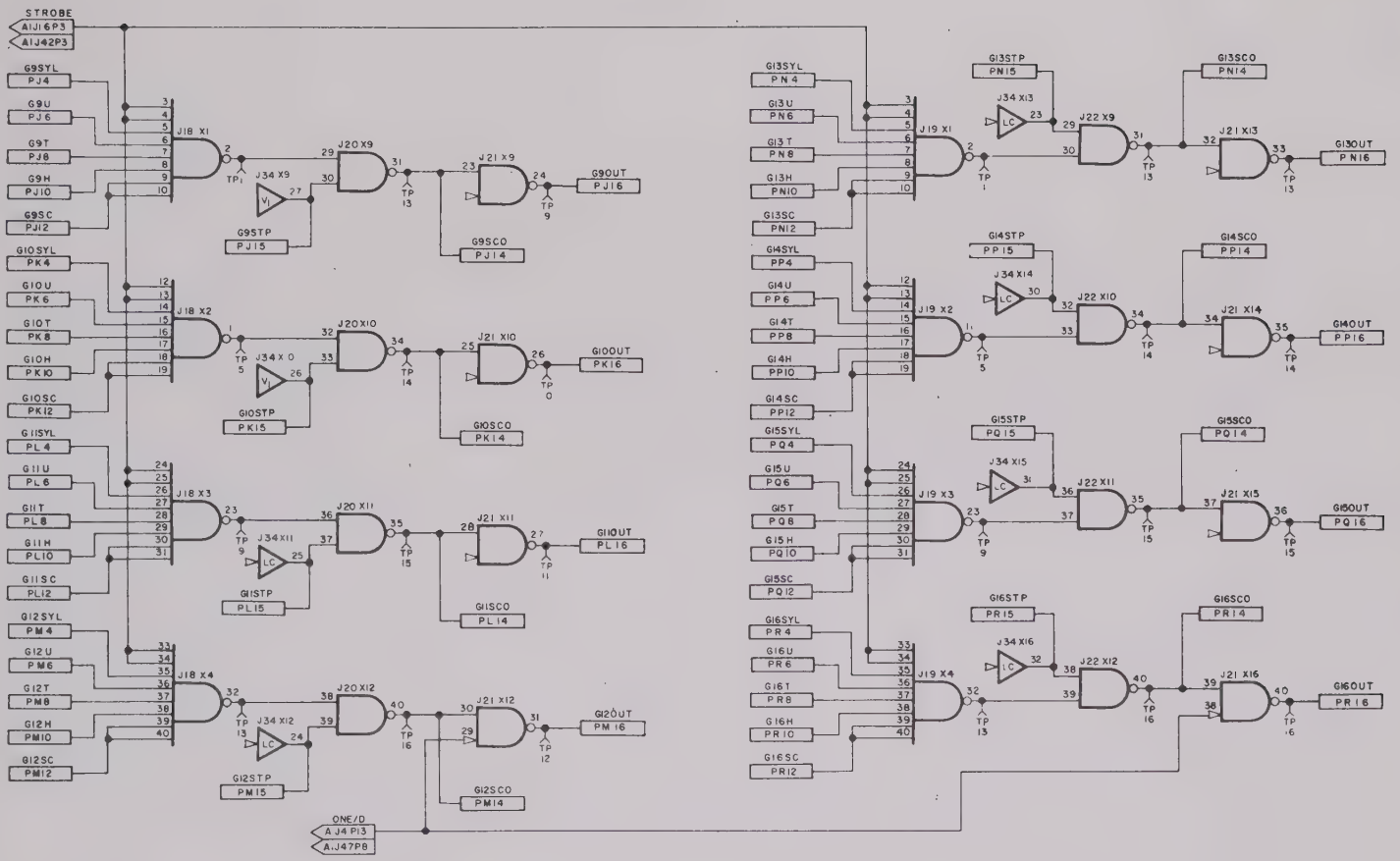
Figure 4-11. Patchboard Shunts



NOTES

1. ALL LOGIC SYMBOL JACK AND CIRCUIT NUMBERS (J__X__) ARE PREFIXED BY A1 UNLESS OTHERWISE INDICATED
2. ALL PIN NUMBERS APPEARING IN RECTANGULAR FLAGS (P___) ARE PREFIXED BY A6 UNLESS OTHERWISE INDICATED
3. FMR DRAWING NO. 7478 (SHEET 1 OF 4)

Figure 4-12. Collection Gates, Logic Diagram (Sheet 1 of 4)



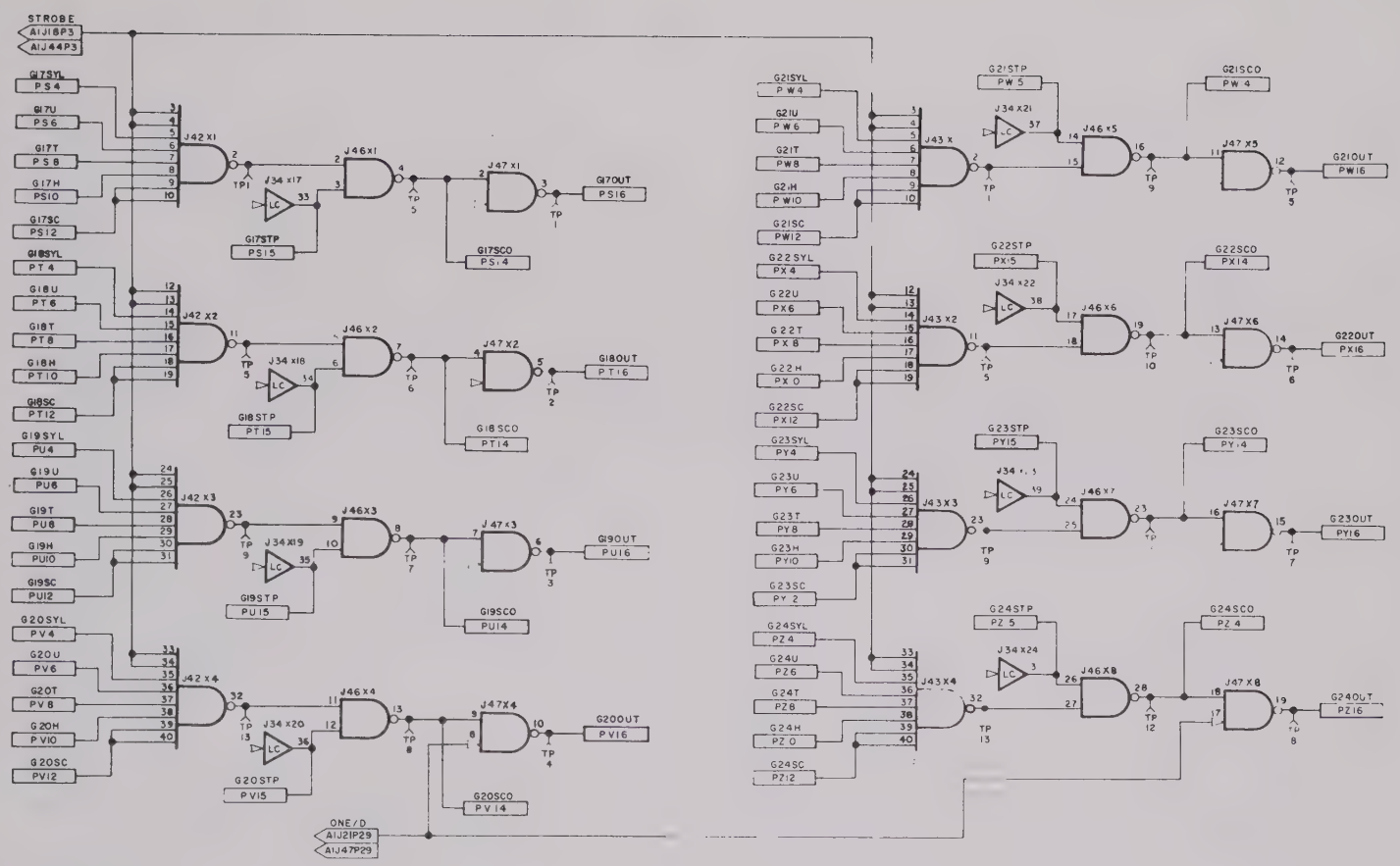
3. EMR DRAWING NO. 7470 (SHEET 2 OF 4)

2 ALL PIN NUMBERS APPEARING IN RECTANGULAR FLAGS (P____) ARE PREFIXED BY A6 UNLESS OTHERWISE INDICATED

1 ALL LOGIC SYMBOL JACK AND CIRCUIT NUMBERS (J__X__) ARE PREFIXED BY A1 UNLESS OTHERWISE INDICATED

NOTES

Figure 4-12. Collection Gates, Logic Diagram (Sheet 2 of 4)



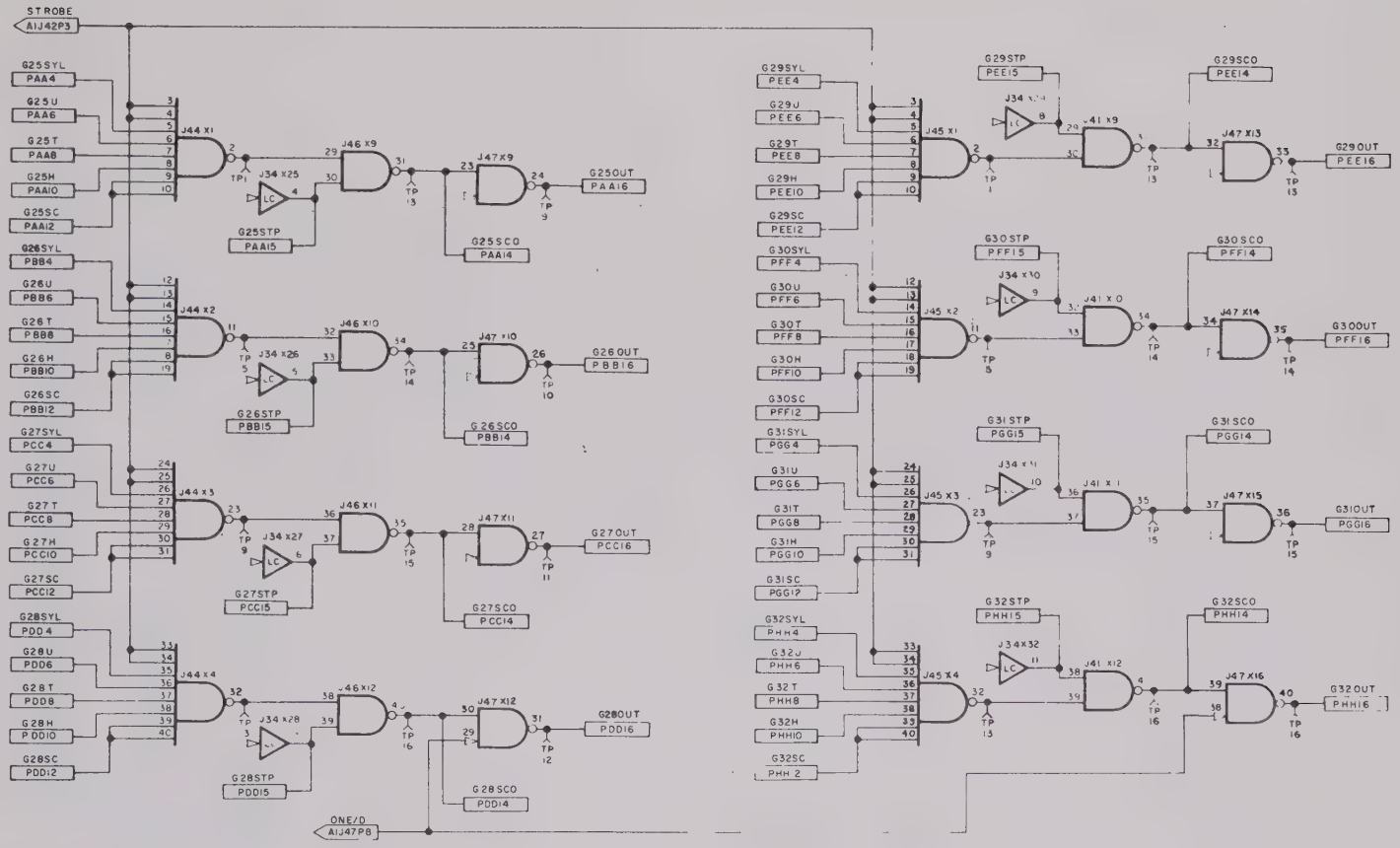
3. EMR DRAWING NO. 7478 (SHEET 3 OF 4)

2 ALL PIN NUMBERS APPEARING IN RECTANGULAR FLAGS (P___) ARE PREFIXED BY A 6 UNLESS OTHERWISE INDICATED

1. ALL LOGIC SYMBOL JACK AND CIRCUIT NUMBERS J___X___ ARE PREFIXED BY A1 UNLESS OTHERWISE INDICATED

NOTES

Figure 4-12. Collection Gates, Logic Diagram (Sheet 3 of 4)



3. ENR DRAWING NO. 7478 (SHEET 4 OF 4)

2. ALL PIN NUMBERS APPEARING IN RECTANGULAR FLAGS (P___) ARE PREFIXED BY A6 UNLESS OTHERWISE INDICATED

1. ALL LOGIC SYMBOL JACK AND CIRCUIT NUMBERS ___ ARE PREFIXED BY A1 UNLESS OTHERWISE INDICATED

NOTES

Figure 4-12. Collection Gates, Logic Diagram (Sheet 4 of 4)

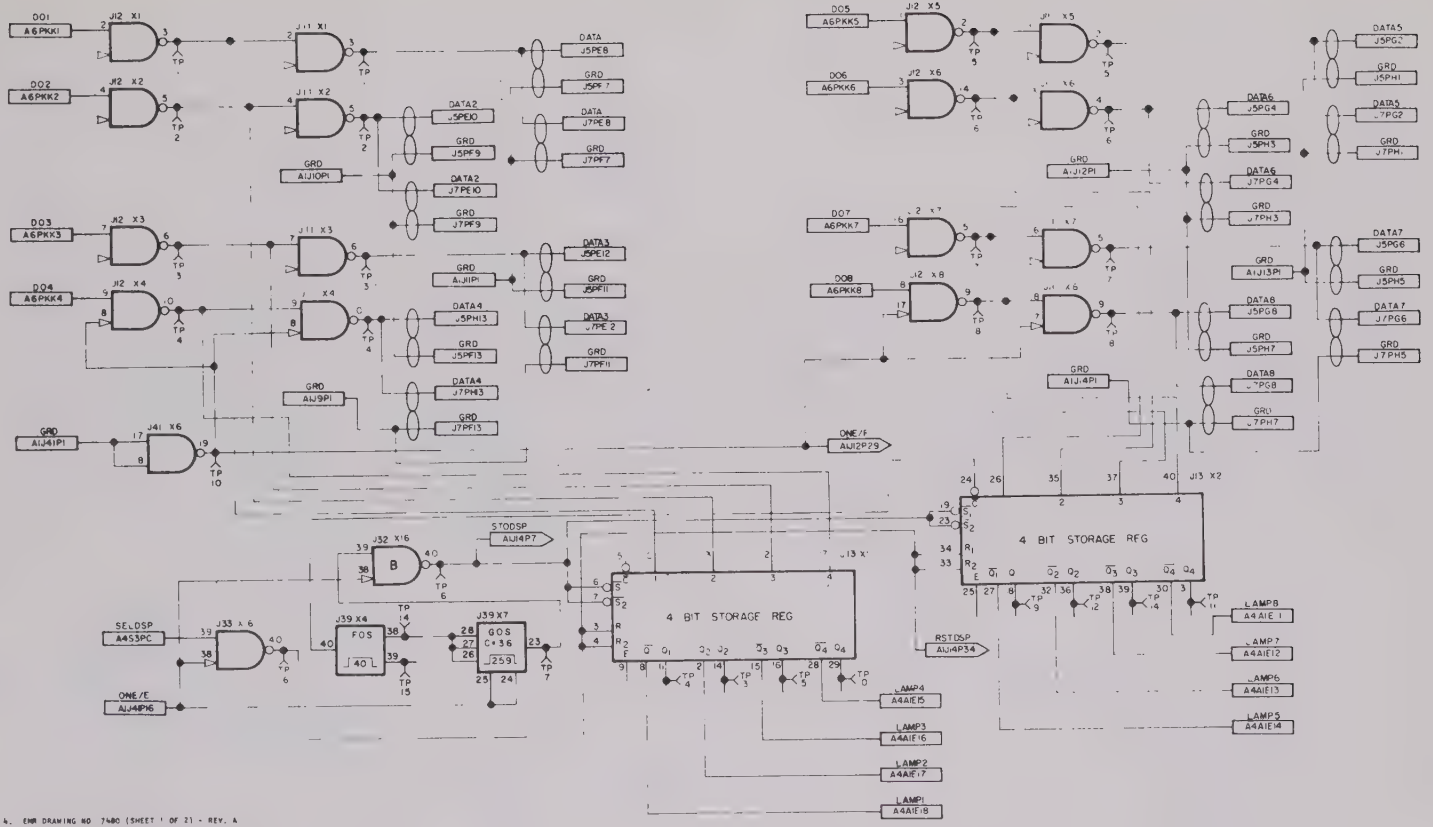
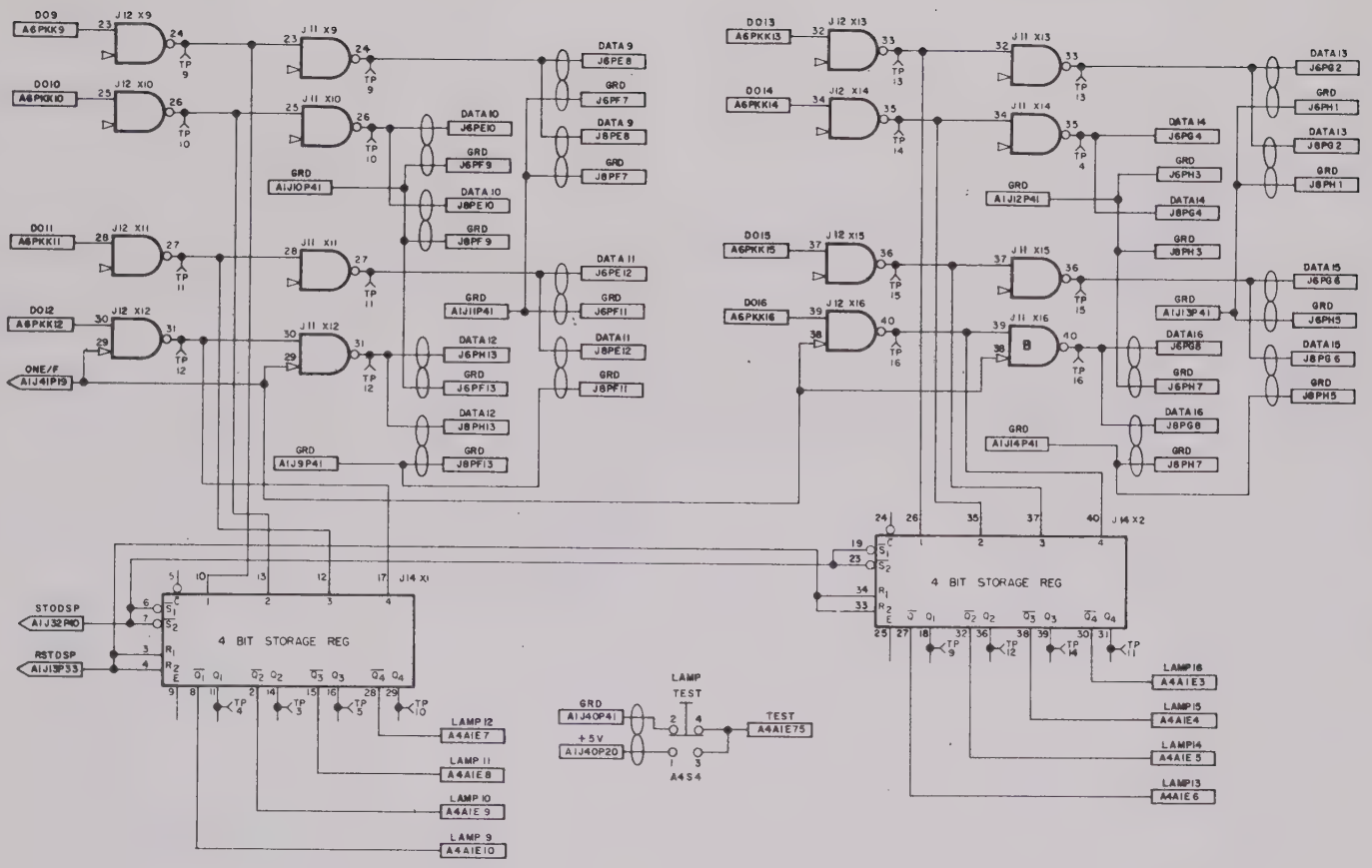

4 BIT STORAGE REG
4 BIT STORAGE REG
NOTES
1. ALL LOGIC SYMBOL JACK AND CIRCUIT NUMBERS (J__X__) ARE PREFIXED BY A1 UNLESS OTHERWISE INDICATED
2. ALL JACK AND PIN NUMBERS (J__P__) APPEARING IN FLAGS ARE PREFIXED BY A5 UNLESS OTHERWISE INDICATED
3. ONE SHOT: TIME IS EXPRESSED IN NSEC AND C IN PF UNLESS OTHERWISE INDICATED
4. ENR DRAWING NO 7480 (SHEET 1 OF 2) - REV. A

Figure 4-13. Data Display and Output Buffers, Logic Diagram (Sheet 1 of 2)



3. EMR DRAWING NO. 7480 (SHEET 2 OF 2)

2 ALL JACK AND PIN NUMBERS (J__P__) APPEARING IN FLAGS ARE PREFIXED BY A5 UNLESS OTHERWISE INDICATED

1 ALL LOGIC SYMBOL JACK AND CIRCUIT NUMBERS (J__X__) ARE PREFIXED BY A1 UNLESS OTHERWISE INDICATED

NOTES

Figure 4-13. Data Display and Output Buffers, Logic Diagram (Sheet 2 of 2)

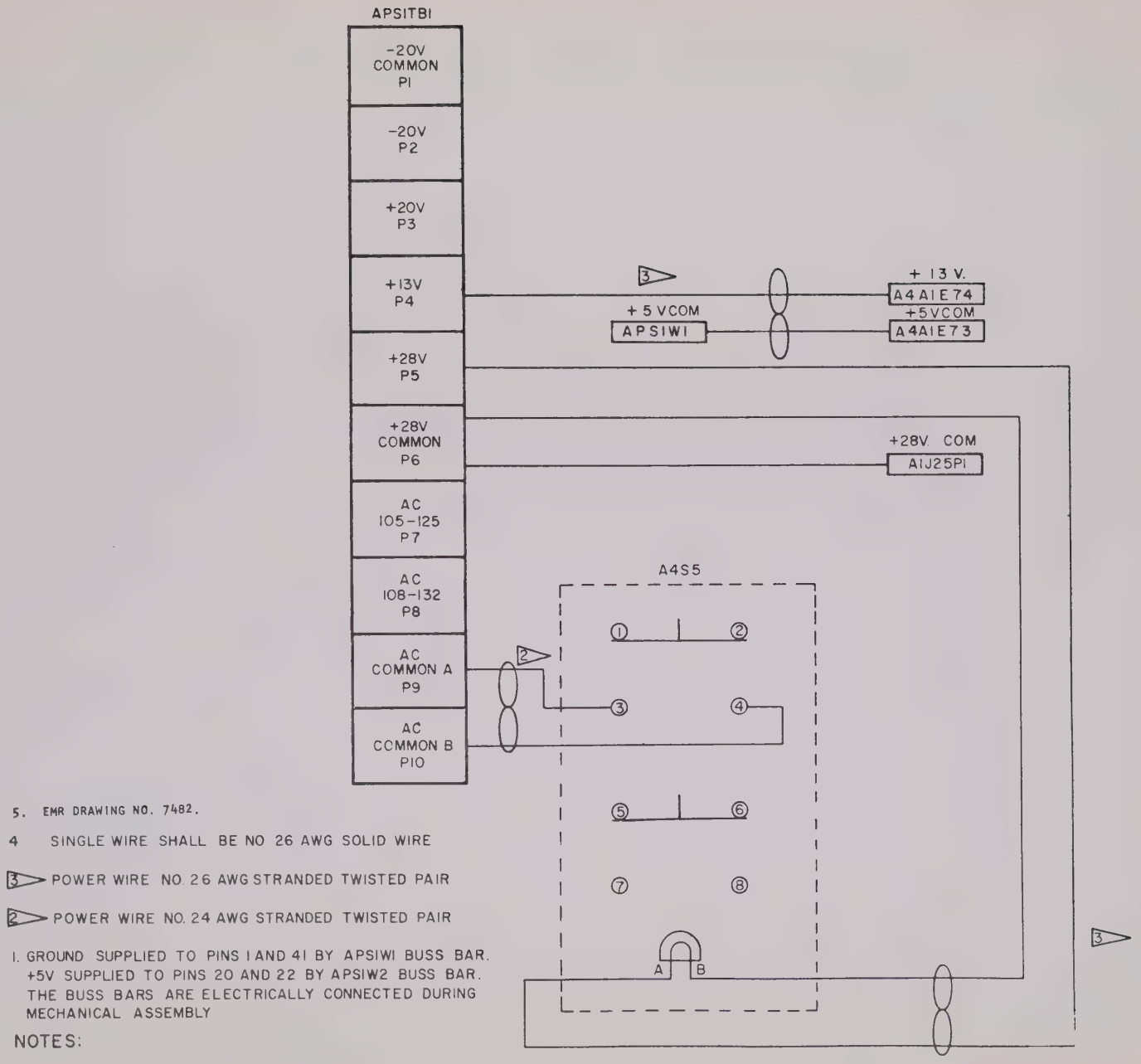
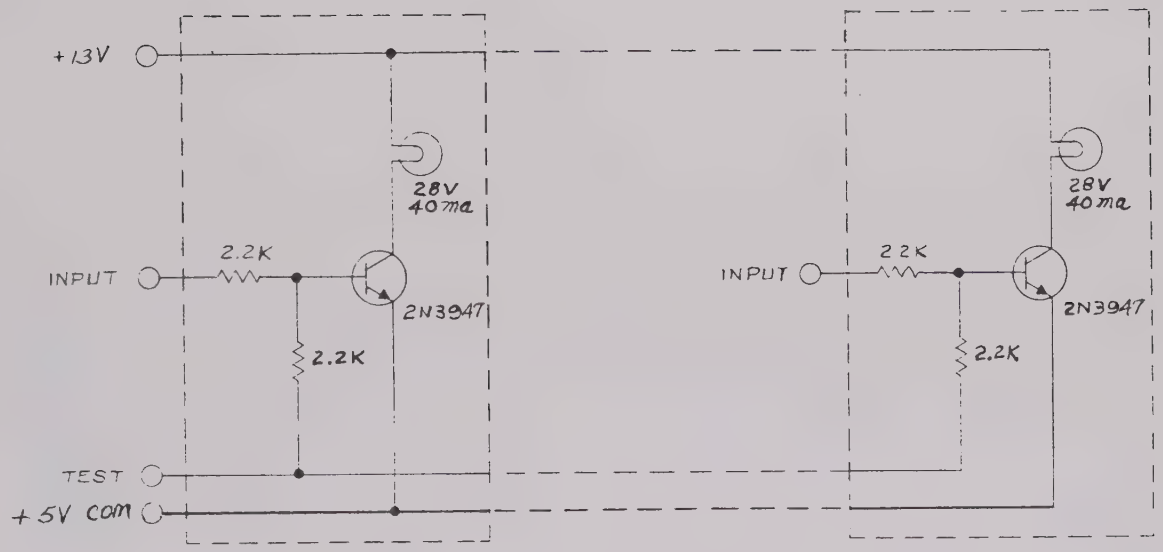


Figure 4-14. Power Distribution Diagram



NOTE:

1. ALL RESISTOR VALUES ARE IN OHMS (K=1000) ±5%, 1/4 WATT.
2. ALL COMPONENT VALUES AND TYPES ARE TYPICAL FOR ALL CIRCUITS.
3. EMR DRAWING NO. 8726.

Figure 4-15. Display Card Schematic

Table 4-1. Mnemonic Descriptions

MNEMONIC	DESCRIPTION
ADRn	Channel transfer outputs (1-32).
DATAn	Data outputs (1-16).
DOn	Patchable data bits (1-16).
FRATE	Frame rate pulse from external source.
FR1CLK	Pulse used to clock Frame Counter No. 1.
FR1Hn	Hundreds outputs (0-5) from Frame Counter No. 1.
FR1RST	Pulse used to reset Frame Counter No. 1.
FR1Tn	Tens outputs (0-9) from Frame Counter No. 1.
FR1Un	Units outputs (0-9) from Frame Counter No. 1.
FR2EN	Signal which enables clock and reset lines to Frame Counter No. 2 for operation with Models 2730/2735.
FR2Hn	Hundreds outputs (0-5) from Frame Counter No. 2.
FR2Tn	Tens outputs (0-9) from Frame Counter No. 2.
FR2Un	Units outputs (0-9) from Frame Counter No. 2.
GnH	Hundreds words or frames count (1-32) to Collection Gates
GnOUT	Collection Gate outputs (1-32).
GnSC	Subcommutation input (1-32) to Collection Gates.
GnSCO	Subcommutation output (1-32) of Collection Gates which may be used as GnSC input to other Collection Gates.
GnSTP	Strapping inputs (1-32) to Collection Gates.
GnSYL	Syllable count inputs (1-32) to Collection Gates.

Table 4-1 (Cont'd.). Mnemonic Descriptions

MNEMONIC	DESCRIPTION
GnT	Tens words or frames count (1-32) to Collection Gates.
GnU	Units words or frames count (1-32) to Collection Gates.
INBn	Inputs (1-10) to Buffer Gates.
LAMPn	Patchable data bits (1-16) that can be displayed on front panel.
nTENS	Tens switch outputs (0-3) used in conjunction with units switch outputs to determine system output to be displayed on front panel.
ONE/A through ONE/F	ONE sources used to tie off unused inputs.
OUTBn	Outputs (1-10) of Buffer Gates.
OUTDRQ	Output Data Request line from Model 2710 which is used for WDXFER.
PDINn	Parallel data inputs (1-16) to the patchboard.
PDOn	Parallel data outputs (1-16) (Inputs to 2745).
RSTDSP	A 72 ns display reset pulse used to reset the Front Panel Display Register.
SELDSP	Display Selection of 1 of the 32 system output lines.
SFINC 1	Subframe Increment pulse from Models 2730/2735 or 2746.
SFINC 2	Subframe Increment pulse from Models 2730/2735.
SFRS 1	Subframe Reset pulse from Models 2730/2735/2746.
SFRS 2	Subframe Reset pulse from Models 2730/2735.

Table 4-1 (Cont'd.). Mnemonic Descriptions

MNEMONIC	DESCRIPTION
START	Used to generate STROBE.
STODSP	Used to gate the data into the Data Display storage register.
STROBE	A 259 ns pulse used as a data transfer command.
SYCLK	A 40 ns pulse used to clock the Syllable Counter and used via START to generate STROBE.
SYLn	Syllable count outputs (1-4).
SYPRS	Word rate pulse used to generate Syllable Counter preset.
SYRATE	Syllable rate pulse from Model 2730.
SYXFER	Used to generate SYLCLK when receiving inputs from Model 2730. Binary 1 when receiving inputs from Models 2710 or 2746.
TEST	Voltage level used to test all front panel lights.
WDCLK	Word rate pulse used in generating STROBE.
WDHn	Hundreds outputs (0-5) from Word Counter.
WDRATE	Word rate pulse from Model 2710 or Model 2730.
WDRST	Frame rate pulse used to generate the word counter reset.
WDTn	Tens outputs (0-9) from Word Counter.
WDUn	Units outputs (0-9) from Word Counter.
WDXFER	Word Transfer pulse used to generate WDCLK.

SECTION 5

MAINTENANCE

5.1 GENERAL

This section provides troubleshooting and maintenance information for the EMR Model 2745 Data Distributor. The information in this section is intended for use in conjunction with the theory of operation and drawings in Section 4 so that maintenance may be performed with maximum efficiency.

In the event of a malfunction, the following general method of troubleshooting and repairing is recommended:

a. Perform a visual inspection in accordance with paragraph 5.2.

b. Perform test procedures in accordance with paragraph 5.3 to aid in isolating the malfunction.

c. After isolating a malfunction to a particular circuit, proceed with normal troubleshooting techniques to locate the defective component using the printed-circuit card schematic diagrams in Section 7. The physical location of components referenced in these schematics are shown in the layout drawings for each card.

d. Refer to Section 6 for component descriptions and identification information.

e. If the malfunction is isolated to the Model 2650 Power Supply, refer to that instruction manual for detailed test procedures.

5.2 INSPECTION

The Model 2745 Data Distributor should be subject to regular periodic inspections to ensure continued proper operation. The following inspection is recommended as a means of preventive maintenance and as an aid in isolating malfunctions.

a. Inspect chassis and card connectors for signs of damage.

b. Inspect wiring for loose or broken connections.

c. Inspect printed-circuit cards for physical damage and component discoloration caused by overheating.

d. Ensure that all printed-circuit cards are firmly seated.

e. Inspect power supply assembly for physical damage and component discoloration caused by overheating.

f. Inspect air intake and exhaust grills and the blower for dust, dirt, or foreign matter which may impede airflow.

CAUTION

Serious damage to the unit may result if the air flow is impeded.

5.3 TEST PROCEDURES

The data and timing signals from the selected input source should be verified before performing test procedures on the Model 2745. The procedures listed below are provided as a general guide for troubleshooting the unit.

a. Apply power to unit and check all power supply voltages at APS1TB1 (Figure 4-14) as follows:

Test Point on APS1TB1	Meter Reading	
P1 (-20V Common)	0V	
P2 (With respect to P1)	-20V ±0.2V	
P3	+20V ±0.2V	
P4	≈ +13V	
P5	≈ +28V	
P6 (Ground)	0V	
P7 (With respect to P9)	AC line voltage	Refer to Paragraph 2.2.6
P8 (With respect to P9)	AC line voltage	
P9 (AC common)	0V	
P10 (AC common)	0V	

b. Check +5V bus bar (APS1W2) and ground bus bar (APS1W1) for proper indications (+5V ±0.15V and ground, respectively).

c. If any reading in steps a and b is out of tolerance, perform detailed test procedures provided in Model 2650 Power Supply manual.

d. On front panel depress LAMP TEST pushbutton switch and note that all DATA lamps light.

e. Remove power and insert printed circuit cards in card file assembly A1.

f. Apply power to unit and connect data and timing input source to proper input connector at rear panel connector assembly A5.

g. Set INPUT switch to position corresponding to input source.

h. Check syllable, word and frame counter outputs at top of patchboard (red area).

i. Check data display circuits by patching a word count from word counter outputs to the corresponding inputs of a selected collection gate, and patching COLLECTION GATE OUTPUT to corresponding SYSTEM OUTPUT.

j. Set the DISPLAY SELECT switches to the selected collection gate number and observe that correct data is displayed.

k. Check buffers as follows:

    1. Patch word count from word counter outputs to a selected collection gate input.

    2. Patch COLLECTION GATE OUTPUT of selected collection gate to BUFFERS IN 1 at bottom of patchboard.

    3. Strap the buffers by patching from BUFFER OUT 1 to BUFFER 2 IN, etc. and patch BUFFER 10 OUT to SYSTEM OUTPUT.

    4. Set DISPLAY SELECT to number of selected system output and observe that correct data is displayed. Malfunction of any buffer may be isolated in this manner.

l. Check collection gates as follows:

    1. With no patching, check all COLLECTION GATE outputs at the patchboard. The output of each gate should be a 259 ns ±10% negative-going (logic ZERO) pulse at the word (or syllable) rate.

    2. Check each collection gate output by patching a syllable count (if Model 2730 is used as the input source) and word count to each collection gate input and monitoring the collection gate output. The output of each collection gate should be a 259 ns ±10% negative-going (logic ZERO) pulse when the proper word count occurs.

m. Check collection gate strapping by performing procedures in paragraph 3.2.2.3 and observing output of last collection gate in the chain. Observe that each gate is in the series chain by breaking the chain at each strapped gate. For this test, a logic ZERO should be patched into one of the inputs of each collection gate except Gate 1.

SECTION 6

REPLACEABLE PARTS LIST AND RECOMMENDED SPARES

6.1 GENERAL

This section contains a tabular listing, (Table 6-1) by major assembly, of electrical and mechanical parts in the Model 2745 Data Distributor. A detailed component listing of each printed wiring assembly (card) in the unit is included with the individual card description in Section 7.

Each major assembly in the DESCRIPTION column of Table 6-1 is identified by an A (assembly) designation in the REF. DESIG. column. (The physical location of each major assembly is shown in Figure 1-1.) Other columns in Table 6-1 include EMR Stock Number, Manufacturers' Code (identified in Table 6-2), Manufacturers' Part Number, Total Quantity (TQ) used in the unit, and Recommended Spares (RS). The recommended spares as listed in Table 6-1 are based on the following listed conditions: (Paragraph 6.2 describes various other considerations for use as an aid in determining individual provisioning requirements.)

1. Operating time -- 8 hours/day, 5 days/week (2080 hours/year).
2. Operating temperature -- 0°C to 30°C.
3. User has capability to repair to the component level.
4. Failure rates are constant.
5. A 0.9 probability of being able to repair from the recommended complement for one year.
6. Equipment will be used as ground equipment (as opposed to vehicular or airborne).

The electrical parts listed at the end of Table 6-1 are the recommended spare parts for the printed circuit cards not recommended to be spared at the card level.

6.2 PROVISIONING CONSIDERATIONS

The selection of an optimum spare parts complement involves a number of considerations known only to the user. These considerations include operating time and cycles, operating environment, number of equipments to be spared and their locations with respect to one another, urgency of returning an equipment to service, troubleshooting, repair and test capability, stock of commonly used parts, etc.

Sparing considerations known to EMR include mean-time-between-failures for parts and assemblies under various operating environments, prices, relative ease of troubleshooting, repair, retest, etc.

Table 6-3 lists the type of information required in order for EMR to recommend an optimum spare parts complement for specific operating and logistic situations.

If the information outlined in Table 6-3 is supplied to EMR, a recommended list will be furnished at no cost for each individual situation.

6.3 ORDERING INSTRUCTIONS

When ordering parts, complete description of each part as listed in DESCRIPTION column of parts list must accompany order. Also included, must be the EMR stock number and manufacturers' name and part number.

Table 6-1. Model 2745 Parts List

REF. DESIG.	DESCRIPTION	EMR STOCK NO.	MFGR. CODE	MFGR. PART NO.	TQ	RS	UNIT PRICE
	DATA DISTRIBUTOR ASSY.	417-89-00001	06141	11171	1	--	Price and delivery of recommended spares on request.
	CONNECTOR FILE ASSY.	112-89-00007	06141	11160	1	--	
A1	RECEPTACLE ASSY., Model 2620	063-95-00001	06141	7350	1	--	
A6	PATCH PANEL ASSY.	191-89-00074	06141	7488	1	--	
A4	SUBPANEL ASSY.	191-89-00076	06141	11163	1	--	
S1	SWITCH, Rotary	250-98-00061	71450	212-20153-6	1	--	
S2	SWITCH, Rotary	250-98-00062	71450	212-19927-4	1	--	
S3	SWITCH, Rotary	250-98-00063	71450	212-19928-1	1	--	
S4	SWITCH, Button, Miniature	250-98-00021	07137	MSB-C-BT4	1	--	
S5	SWITCH, Pushbutton, Lited	250-98-00044	97564	1160A7L56W 1-L	1	--	
	LAMP, T, 1 3/4, 28V	151-02-00001	G81349	MS25237-327	1	--	
A4A1	PRINTED WIRING ASSY., DISPLAY CARD	205-89-00153	06141	8724-3	1	--	
DS1 thru DS16	LAMP, Unbased, 28V, 40 Ma	151-98-00008	71744	CM1764 w/tin dip leads	16	2	
Q1 thru Q16	TRANSISTOR	263-10-39470	JEDEC	2N3947	16	2	
R1 thru R32	RESISTOR, 2.2K, 5%, 1/4W	616-02-22000	QPL-11*	RC07GF222J	32	3	
	FRONT PANEL ASSY.	191-89-00075	06141	7468	1	--	
	LENS, Clear Amber	154-98-00001	03797	110-10988-204	16	--	
A5	CONNECTOR PLATE ASSY.	196-89-00009	06141	11155	1	--	
J1 thru J8	RECEPTACLE, Miniature, 52-Pin	063-98-00063	13511	220-2N052	8	--	
P1 thru P8	PLUG, Miniature, 52-Pin	063-98-00056	13511	220-1N052	8	--	
PS1	POWER SUPPLY, Model 2650	202-95-00001	06141	7390	1	--	
	PRINTED WIRING ASSY., Model 2501	205-95-00001	06141	4001	6	--	

*Qualified Products List of Qualified Products Under MIL-R-11

Table 6-1 (Cont'd.). Model 2745 Parts List

REF. DESIG.	DESCRIPTION	EMR STOCK NO.	MFGR. CODE	MFGR. PART NO.	TQ	RS	UNIT PRICE
	PRINTED WIRING ASSY., Model 2502	205-95-00002	06141	4002	1	--	
	PRINTED WIRING ASSY., Model 2503	205-95-00003	06141	4003	4	--	
	PRINTED WIRING ASSY., Model 2506	205-95-00006	06141	4006	8	--	
	PRINTED WIRING ASSY., Model 2546	205-95-00014	06141	4046	2	--	
	PRINTED WIRING ASSY., Model 2564	205-95-00018	06141	4064	1	--	
	PRINTED WIRING ASSY., Model 2567	205-95-00021	06141	4067	9	1	
	PRINTED WIRING ASSY., Model 2590	205-95-00024	06141	4090	1	--	
	PRINTED WIRING ASSY., Resistor	205-89-00046	06141	8301	1	--	
	PATCH CORD, Shunt, Manual	070-98-00005	*	10350-2	125	--	
	PATCH CORD, 5 in., Red, Manual	070-98-00006	*	10342-2	75	--	
	PATCH CORD, 7 in., Gry, Manual	070-98-00007	*	10343-2	100	--	
	PATCH CORD, 9 in., Blu, Manual	070-98-00008	*	10344-2	50	--	
	PATCH CORD, 11 in., Grn, Manual	070-98-00009	*	10345-2	25	--	
	KNOB, Dk Green (used on A4S1)	148-99-00005	06141	7370-1	1	--	
	KNOB, lt Green (used on A4S2 & A4S3)	148-99-00007	06141	7370	2	--	
	EXTRACTOR, Circuit Board	280-98-00001	78769	1731	1	--	
	*Cam Corp., Greensboro, N. C.						
	The following listed parts are recommended as spares for the printed-wiring assemblies (cards) in this unit not recommended to be spared at the card level.						
	INTEGRATED CIRCUIT, SF-53-03	046-14-00009	93332	SF-53-03	90	9	
	INTEGRATED CIRCUIT, SG-63-03	046-14-00003	93332	SG-63-03	32	3	
	INTEGRATED CIRCUIT, SG-92-03	046-14-00005	93332	SG-92-03	4	1	
	INTEGRATED CIRCUIT, SG-142-03	046-14-00006	93332	SG-142-03	17	2	
	INTEGRATED CIRCUIT, SG-143-03	046-14-00007	93332	SG-143-03	50	5	
2564	CAPACITOR, 100 pf, ±10%, 200V	347-03-10009	06141		8	1	
8301	RESISTOR, 1.6K, ±10%, 1/2 W	622-03-16000	01121	RC20GF162K			
2564	RESISTOR, 3.9K, ±5%, 1/4W	616-02-39000	G81349	RC07GF392J			
2564	RESISTOR, 10K, ±5%, 1/4W	616-02-10001	G81349	RC07GF103J			
2564	TRANSISTOR, 2N2475/46	263-14-24758	93332	2N2475/46			

Table 6-2. Manufacturers' Names and Code Numbers

MFR'S CODE	MFR'S NAME AND ADDRESS
01121	Allen-Bradley Co., Milwaukee, Wis.
03797	Eldema Corp., Compton, Calif.
05170	Engineered Electronics Co., Inc., Santa Ana, Calif.
06141	Electro-Mechanical Research, Inc., Sarasota, Fla.
07137	Transistor Electronics Corp., Minneapolis, Minn.
07716	IRC, Inc., Burlington, Iowa
09353	C and K Components, Inc., Newton, Mass.
13511	Amphenol Corp., Los Gatos, Calif.
71450	CTS Corp., Elkhart, Ind.
71744	Chicago Miniature Lamp Works, Chicago, Ill.
74970	E. F. Johnson Co., Waseca, Minn.
78769	E. H. Titchener and Co., Binghamton, N. Y.
G81349	Military Specifications promulgated by Standardization Div. Directorate of Logistic Services DSA
93332	Sylvania Electric Products, Inc., Woburn, Mass.
97564	Clare-Pendar, Inc., Post Falls, Idaho

Table 6-3. Customer Provisioning Questionnaire

1.	Equipment to be spared Model No.(s): _____ Serial No.(s): _____
2.	Number of equipments to be spared in each location _____
3.	Operating time and cycle: _____ hours/day, _____ days/ week.
4.	Operating Environment: A. Temperature: _____ B. Humidity: _____ C. Altitude: _____ D. Shock and Vibration: _____
5.	Non-operating Environment: _____ A. Temperature: _____ B. Humidity: _____ C. Altitude: _____
6.	Desired probability of being able to spare from complement _____ percent for _____ months.
7.	Can usage permit troubleshooting to parts level when a failure occurs? _____
8.	What spare assemblies do you have that are used in this Model Equipment? _____
9.	Do you wish us to exclude the EMR warranty period? _____

SECTION 7

EMR PRINTED-WIRING ASSEMBLY DESCRIPTIONS

7.1 GENERAL

This section contains a description of each printed-wiring assembly used in the Model 2745 Data Distributor.

EMR MODEL 2501 16-INVERTER NAND GATES DIGITAL LOGIC CARD

1. DESCRIPTION

The EMR Model 2501 16-Inverter NAND Gates (16-INA) Digital Logic Card contains four SG143 SUHL (Sylvania Universal High Level Logic) integrated-circuit modules. Each SUHL module Z1, Z2, Z3, and Z4 contains four 2-input NAND gates as shown in Figure 1. Each NAND gate is capable of driving six standard loads*. Where a driving capability of up to 12 standard loads* per gate is required, the NAND gates on the identically-configured EMR Model 2502 16-Inverter NAND Buffer Gates (16-INAB) Digital Logic Card are used. Additional applications of the 16-INA Digital Logic Card are discussed in Paragraph 3.

Pins A, E, I, and L on each SUHL module are connected together on the card to provide a common input for simultaneously gating the four individual NAND gate circuits. The gate inputs to SUHL modules Z1, Z2, Z3, and Z4 are applied at card connector pins 8, 17, 29, and 38 respectively. When the common input to each group of four NAND gates is connected to the truth level, each NAND gate in the group functions as an inverter.

2. SPECIFICATIONS

Overall Logic Card specifications are given in Paragraph 2.1 and detailed SUHL Module specifications are presented in Paragraph 2.2. Physical specifications are illustrated in Figure 1.

2.1 Logic Card Specifications

a. Number of Integrated Circuit Modules: 4.
b. Module Type: SG143 SUHL Integrated Circuit.
c. Module Circuit: Four 2-input NAND gates with gating inputs connected together on card.
d. Total Number of Circuits: 16 NAND gates (gated in groups of four).
e. Number of Gating Inputs: 4.
f. Number of Logic Inputs: 16.
g. Number of Outputs: 16.
h. Output Polarity: Inverted.
i. Supply Voltage: +5.0 ±0.25V.
j. Supply Current: 64 Ma.
k. Operating Temperature: 0°C to 75°C.

2.2 SG143 SUHL Integrated Circuit Module Specifications

a. Input Specifications:

(1) Gating Input:

(a) Number: 1.
(b) Input Impedance: 4 standard loads*.
(c) Maximum Input Voltage: +5.5V (logic ONE).
(d) Input Levels:
Logic ONE = +3.0V (+1.9 to 5V)
Logic ZERO = 0V (0 to 1.1V)

(2) Logic Inputs:

(a) Number: 4.
(b) Input Impedance: 1 standard load*.
(c) Maximum Input Voltage: +5.5V (logic ONE).
(d) Input Levels:
Logic ONE = +3.0V (+1.9 to +5V)
Logic ZERO = 0V (0V to +1.1V)

b. Output Specifications:

(1) Number of Outputs: 4.
(2) Output Rise Time: 5 nanoseconds maximum per gate loaded with 6 standard loads* having a total capacitive load of 15 Pf.
(3) Output Fall Time: 8 nanoseconds maximum per gate when loaded with 6 standard loads* having a total capacitive load of 15 Pf.
(4) Average Propagation Delay: 20 nanoseconds maximum per gate when loaded with 6 standard loads* having a total capacitive load of 15 Pf.
(5) Drive Capability: Each gate can drive a maximum of 6 standard loads* having a total capacitive load of 600 Pf.
(6) Output Voltage Swing:
Logic ZERO: 0V to 0.45V.
Logic ONE: +3 to +5V.
(7) Short Circuit Protection: An output may be shorted to ground with no permanent degradation of the circuit.

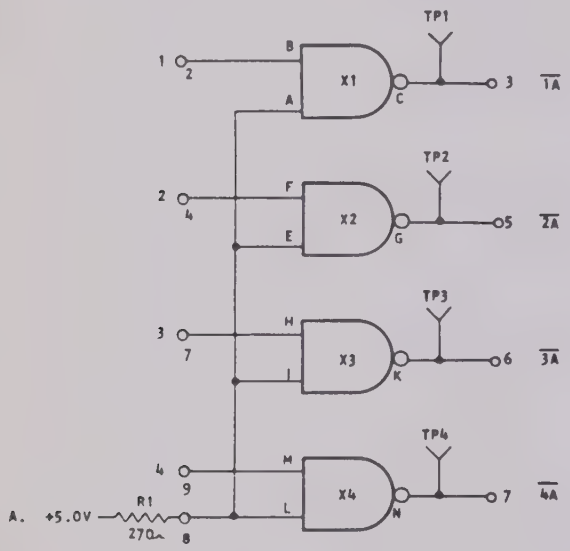
* A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.

3. LOGIC CIRCUIT APPLICATIONS

Typical applications for the circuits included on the EMR Model 2501 16-INA Digital Logic Card are described in the following paragraphs.

3.1 Inversion

When the gate input to the integrated circuit shown in the following figure is connected to the truth level (logic ONE), each of the four NAND gates within the integrated circuit module functions as an inverter.

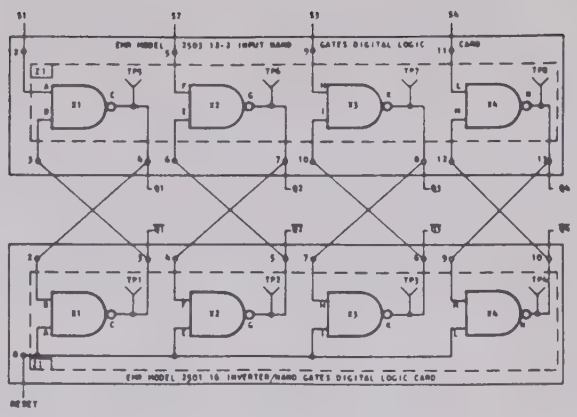


Inverter NAND Gates

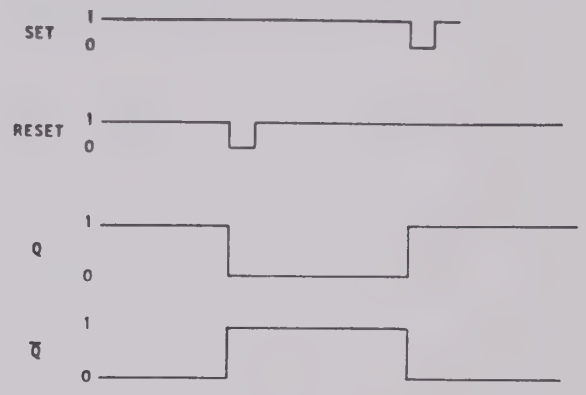
3.2 Flip-Flop Configuration

When the four NAND gates comprising a module on the 16-INA Digital Logic Card are cross-coupled with four NAND gates on the EMR Model 2503 12-2 Input NAND Gates (12-2 NA) Digital Logic Card, as shown in the following figure, a group of four flip-flops is created having a common reset input.

Each pair of cross-coupled NAND gates represents a set-reset flip-flop. The set and reset inputs are normally at the logic ONE state and the Q and $\overline{Q}$ outputs are at the ONE and ZERO state respectively. A logic ZERO applied to either the set or reset inputs changes the state of the flip-flop. The accompanying timing diagram illustrates the operation of the



Flip-Flop Configuration



Set-Reset Flip-Flop Timing

flip-flop upon application of set and reset pulse inputs. The minimum width for the set or reset pulse is 40 nanoseconds. The Q and $\overline{Q}$ outputs from each flip-flop are each capable of driving five standard loads. The flip-flop configuration is used when simultaneous reset of a multiple flip-flop store is required. When individual set-reset flip-flops are required, the individual 2-input NAND gates on the Model 2503 12-2 Input NAND Gates (12-2 NA) Digital Logic Card are cross-coupled to create the desired number of set-reset flip-flops.

3.3 NAND Gate Paralleling

Two or more NAND gates may be connected pin-for-pin on inputs and outputs to provide additional loading capability. When a paralleling configuration is used, it is preferable that the NAND gates be in close proximity to each other. For gates that switch infrequently, a maximum of six gates may be paralleled; for NAND gates switching

at maximum frequency, a maximum of three gates may be paralleled. The total loading capability is equal to the sum of the loading capability of the individual NAND gates.

4. MAINTENANCE

Maintenance of the EMR Model 2501 16-INA Digital Logic Card is limited to the replacement of defective SG143 SUHL Integrated Circuit modules. A defective SG143 SUHL Integrated Circuit module is isolated using the EMR Model 2798 Card Test Set and the test procedures outlined in Table 1.

CAUTION

Use minimum heat required to simultaneously loosen the module pins. Excessive heat will lift land area on card.

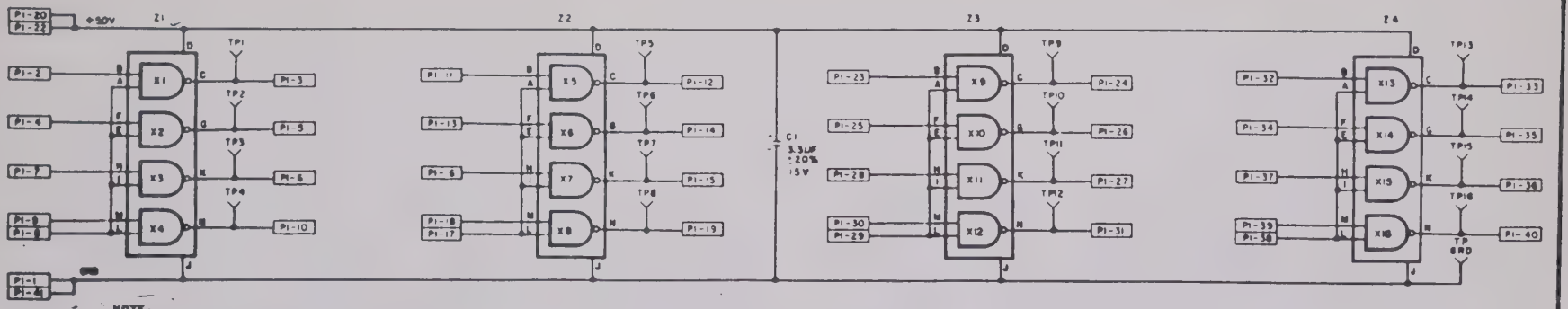
When the defective module has been isolated, the module is removed by simultaneously heating the 14 module contacts on land side of card and withdrawing module from opposite side of card.

The black dot on the replacement module is aligned with the corresponding plated dot on the printed circuit card and the module is inserted into the card. The module contacts are soldered to the plated-through holes on the card using minimum heat and solder.

Table 1. EMR Model 2501 16-Inverter NAND Gates Digital Logic Card Test Procedure

NOTE

Card test procedure provided when EMR Model 2798 Card Test Set is ordered.



NOTE:
IN LOGIC CIRCUIT APPLICATION, COMMON GATE INPUTS TO EACH CIRCUIT OF A MODULE ARE SHOWN WITH AN ARROW (▶) TO INDICATE THE COMMON CONNECTION.

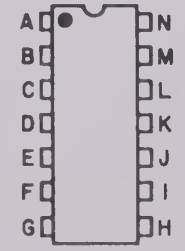
Schematic Diagram

CIRCUIT SYMBOL NO.	DESCRIPTION	MANUFACTURER NAME	MANUFACTURER PART NO
	16 INVERTER NAND GATES PRINTED-WIRING BOARD	EMR	204-99-00001
C1	CAPACITOR, 3.3 µF ±20%, 15V	EMR	336-21-33003
TP GRD	TEST JACK (BLACK)	AUGAT	8041-1G6
TP1 THRU TP16	TEST JACK (BLACK)	AUGAT	8046-1G6
Z1 THRU Z4	INTEGRATED CIRCUIT	SYLVANIA	SG143-03 SUHL

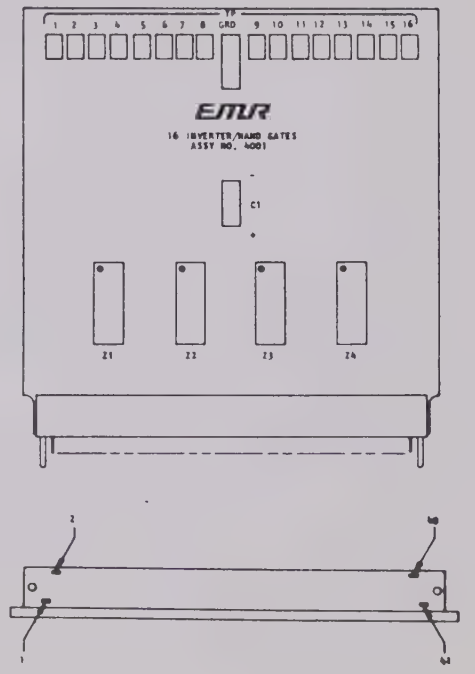
Parts List

A	B	C
1	1	0
1	0	1
0	1	1
0	0	1

Truth Table

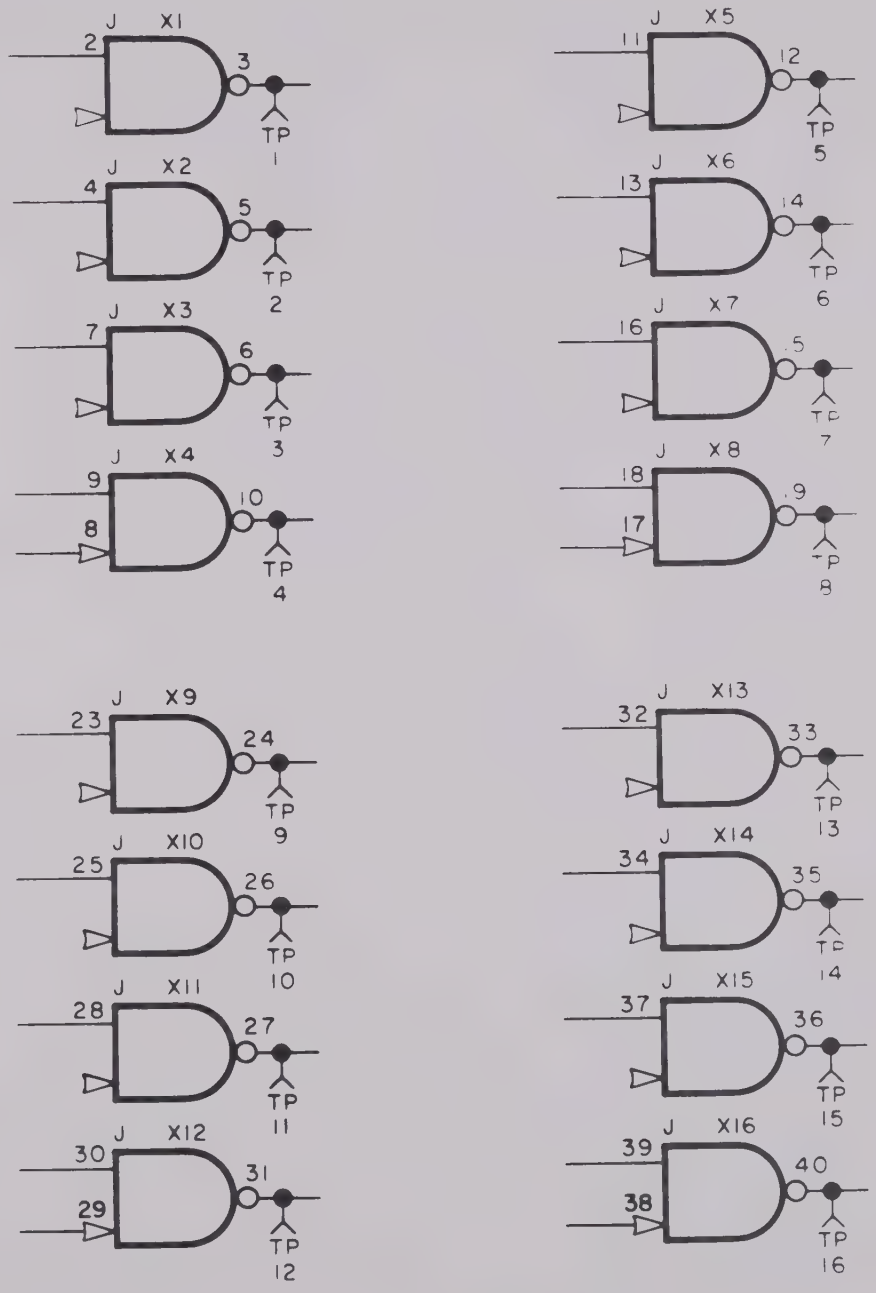


INTEGRATED CIRCUIT
PIN IDENTIFICATION
(TOP VIEW)



Card Layout Diagram

Figure 1 (Sheet 1 of 2)



Logic Symbols

Figure 1 (Sheet 2 of 2)

EMR MODEL 2502 16-INVERTER NAND BUFFER GATES DIGITAL LOGIC CARD

1. DESCRIPTION

The EMR Model 2502 16-Inverter NAND Buffer Gates (16-INAB) Digital Logic Card contains four SG142 SUHL (Sylvania Universal High Level Logic) integrated-circuit modules. Each SUHL module Z1, Z2, Z3, and Z4 contains four 2-input NAND gates as shown in Figure 1. Each NAND gate is capable of driving 12 standard loads*. When a driving capability of only six standard loads* per gate is required, the NAND gates on the identically-configured EMR Model 2501 16-Inverter NAND Gates (16-INA) Digital Logic Card are used. Additional applications of the 16-INAB Digital Logic Card are discussed in Paragraph 3.

Pins A, E, I, and L on each SUHL module are connected together on the card to provide a common input for simultaneously gating the four individual NAND gate circuits. The gate inputs to SUHL modules Z1, Z2, Z3, and Z4 are applied at card connector pins 8, 17, 29, and 38 respectively. When the common input to each group of four NAND gates is connected to the truth level, each NAND gate in the group functions as an inverter.

2. SPECIFICATIONS

Overall Logic Card specifications are given in Paragraph 2.1 and detailed SUHL Module specifications are presented in Paragraph 2.2. Physical specifications are illustrated in Figure 1.

2.1 Logic Card Specifications

a. Number of Integrated Circuit Modules: 4.
b. Module Type: SG142 SUHL Integrated Circuit.
c. Module Circuit: Four 2-input NAND gates with gating inputs connected together on card.
d. Total Number of Circuits: 16 NAND gates (gated in groups of four).
e. Number of Gating Inputs: 4.
f. Number of Logic Inputs: 16.
g. Number of Outputs: 16.
h. Output Polarity: Inverted.
i. Supply Voltage: +5.0 ±0.25V.
j. Supply Current 64 Ma.
k. Operating Temperature: 0°C to 75°C.

2.2 SG142 SUHL Integrated Circuit Module Specifications

a. Input Specifications:

(1) Gating Input:

(a) Number: 1.
(b) Input Impedance: 4 standard loads*.
(c) Maximum Input Voltage: +5.5V (logic ONE.)
(d) Input Levels:
Logic ONE = +3V (+1.9 to 5V)
Logic ZERO = 0V (0 to 1.1V)

(2) Logic Inputs:

(a) Number: 4.
(b) Input Impedance: 1 standard load*.
(c) Maximum Input Voltage: +5.5V (logic ONE.)
(d) Input Levels:
Logic ONE = +3V (+1.9 to +5V)
Logic ZERO = 0V (0V to +1.1V)

b. Output Specifications:

(1) Number of Outputs: 4.
(2) Output Rise Time: 5 nanoseconds maximum per gate loaded with 12 standard loads* having a total capacitive load of 15 Pf.
(3) Output Fall Time: 8 nanoseconds maximum per gate when loaded with 12 standard loads* having a total capacitive load of 15 Pf.
(4) Average Propagation Delay: 20 nanoseconds maximum per gate when loaded with 12 standard loads* having a total capacitive load of 15 Pf.
(5) Drive Capability: Each gate can drive a maximum of 12 standard loads* having a total capacitive load of 600 Pf.
(6) Output Voltage Swing:
Logic ZERO: 0V to 0.45V.
Logic ONE: +3 to +5V.
(7) Short Circuit Protection: An output may be shorted to ground with no permanent degradation of the circuit.

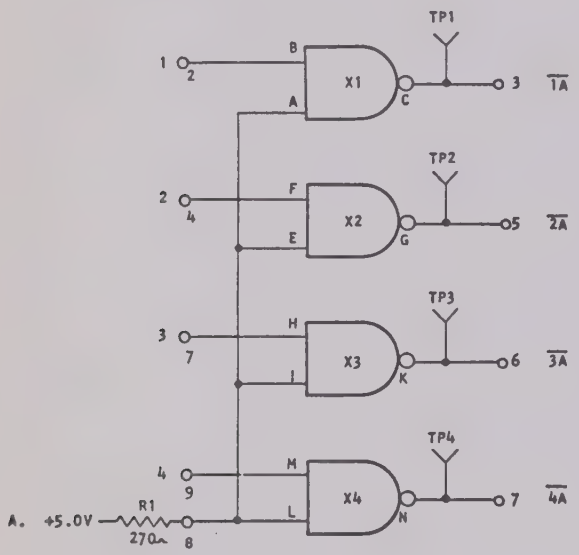
* A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.

3. DIGITAL CIRCUIT APPLICATIONS

Typical applications for the circuits included on the EMR Model 2502 16-INAB Digital Logic Card are described in the following paragraphs.

3.1 Inversion

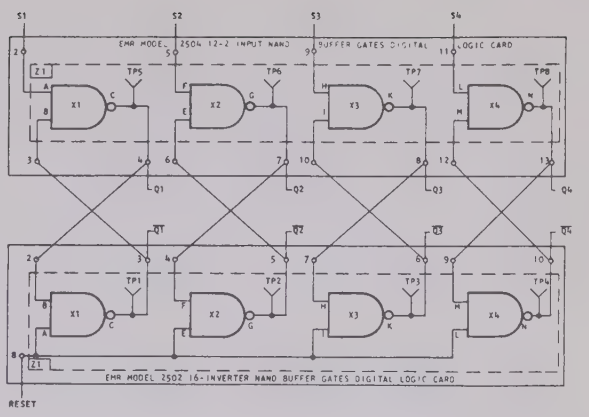
When the gate input to the integrated circuit is connected to the truth level (logic ONE), each of the four NAND gates within the integrated circuit module functions as an inverter.

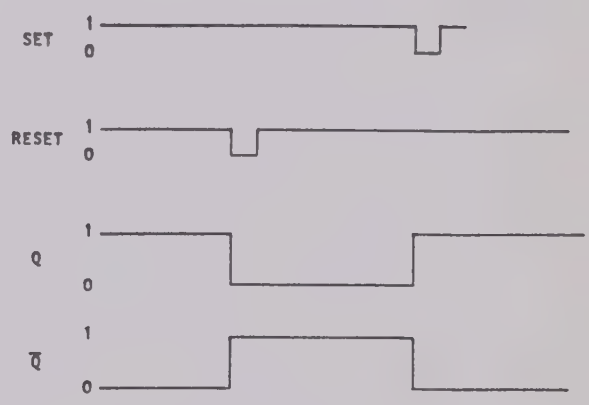


Inverter NAND Gates

3.2 Flip-Flop Configuration

When the four NAND gates comprising a module on the 16-INAB Digital Logic Card are cross-coupled with four NAND gates on the EMR Model 2504 12-2 Input NAND Buffer Gates (12-2NAB) Digital Logic Card, as shown in the following figure, a group of four flip-flops is created having a common reset input.


EMR MODEL 2504 12-2 INPUT NAND BUFFER GATES DIGITAL LOGIC CARD
EMR MODEL 2502 16-INVERTER NAND BUFFER GATES DIGITAL LOGIC CARD
RESET



Each pair of cross-coupled NAND gates represents a set-reset flip-flop. The set and reset inputs are normally at the logic ONE state and the Q and $\overline{Q}$ outputs are at the ONE and ZERO state respectively. A logic ZERO applied to either the set or reset inputs changes the state of the flip-flop. The accompanying timing diagram illustrates the operation of the flip-flop upon application of set and reset pulse inputs. The minimum width for the set or reset pulse is 40 nanoseconds. The Q and $\overline{Q}$ outputs from each flip-flop are each capable of driving 12 standard loads. The flip-flop configuration is used when simultaneous reset of a multiple flip-flop store is required. When individual set-reset flip-flops are required, the individual 2-input NAND gates on the Model 2504 12-2 Input NAND Buffer Gates (12-2NAB) Digital Logic Card are cross-coupled to create the desired number of set-reset flip-flops.

3.3 NAND Gate Paralleling

Two or more NAND gates may be connected pin-for-pin on inputs and outputs to provide additional loading capability. When a paralleling configuration is used, it is preferable that the NAND gates be in close proximity to each other. For gates that switch infrequently, a maximum of six gates may be paralleled; for NAND gates switching

at maximum frequency, a maximum of three gates may be paralleled. The total loading capability is equal to the sum of the loading capability of the individual NAND gates.

4. MAINTENANCE

Maintenance of the EMR Model 2502 16-Inverter NAND Buffer Digital Logic Card is limited to the replacement of defective SG142 SUHL Integrated Circuit modules. A defective SG142 SUHL Integrated Circuit module is isolated using the EMR Model 2798 Card Test Set and the test procedures outlined in Table 1.

CAUTION

Use minimum heat required to simultaneously loosen the module pins. Excessive heat will lift land area on card.

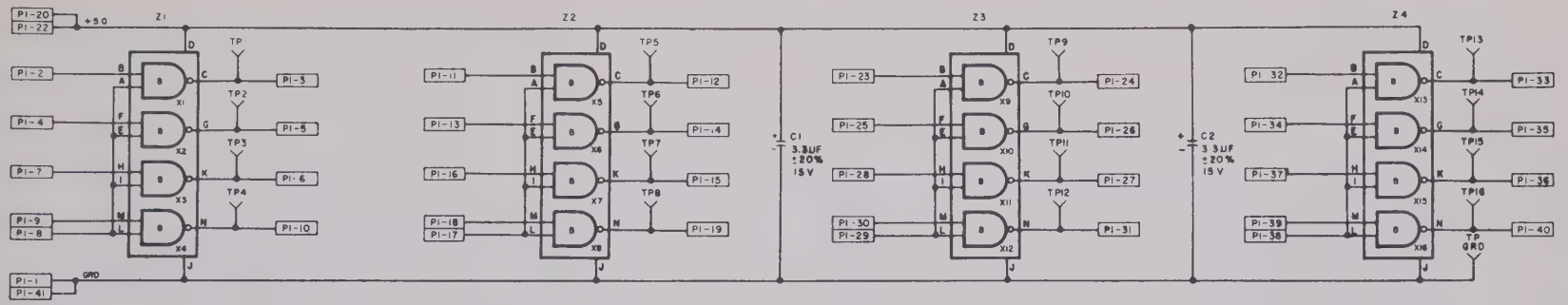
When the defective module has been isolated, the module is removed by simultaneously heating the 14 module contacts on land side of card and withdrawing module from opposite side of card.

The black dot on the replacement module is aligned with the corresponding plated dot on the printed-circuit card and the module is inserted into the card. The module contacts are soldered to the plated-through holes on the card using minimum heat and solder.

Table 1. EMR Model 2502 16-Inverter NAND Buffer Gates Digital Logic Card Test Procedure

NOTE

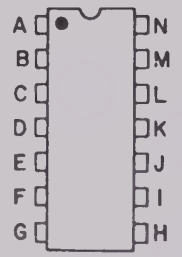
Card test procedure provided when EMR Model 2798 Card Test Set is ordered.



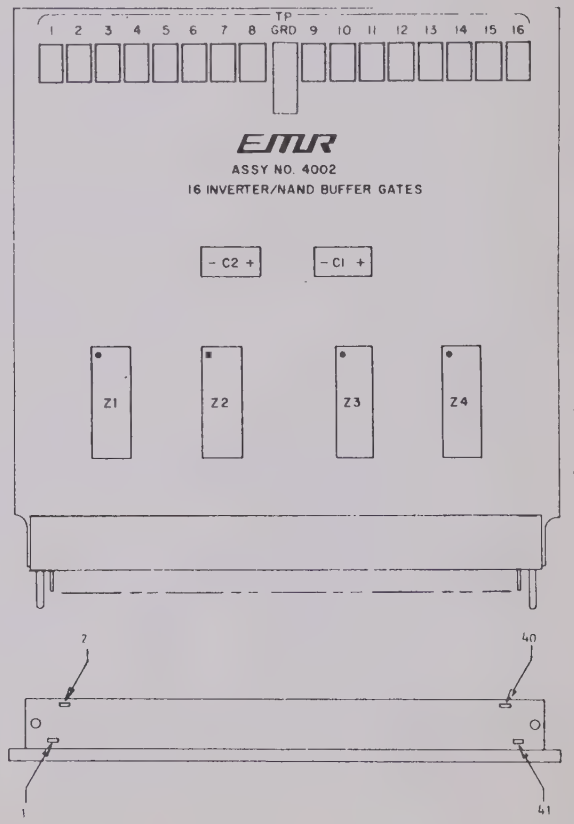
Schematic Diagram

CIRCUIT SYMBOL NO	DESCRIPTION	MANUFACTURER	
		NAME	PART NO
	16 INVERTER NAND BUFFER GATES PRINTED-WIRING BOARD	EMR	204-99-00002
C1 AND C2	CAPACITOR, 3.3 µF ±20%, 15V	EMR	333-21-33003
TP GRD	TEST JACK (BLACK)	AUGAT	8041-1G6
TP1 THRU TP16	TEST JACK (BLACK)	AUGAT	8046-1G6
Z1 THRU Z4	INTEGRATED CIRCUIT	SYLVANIA	SG142-03 SUHL

Parts List

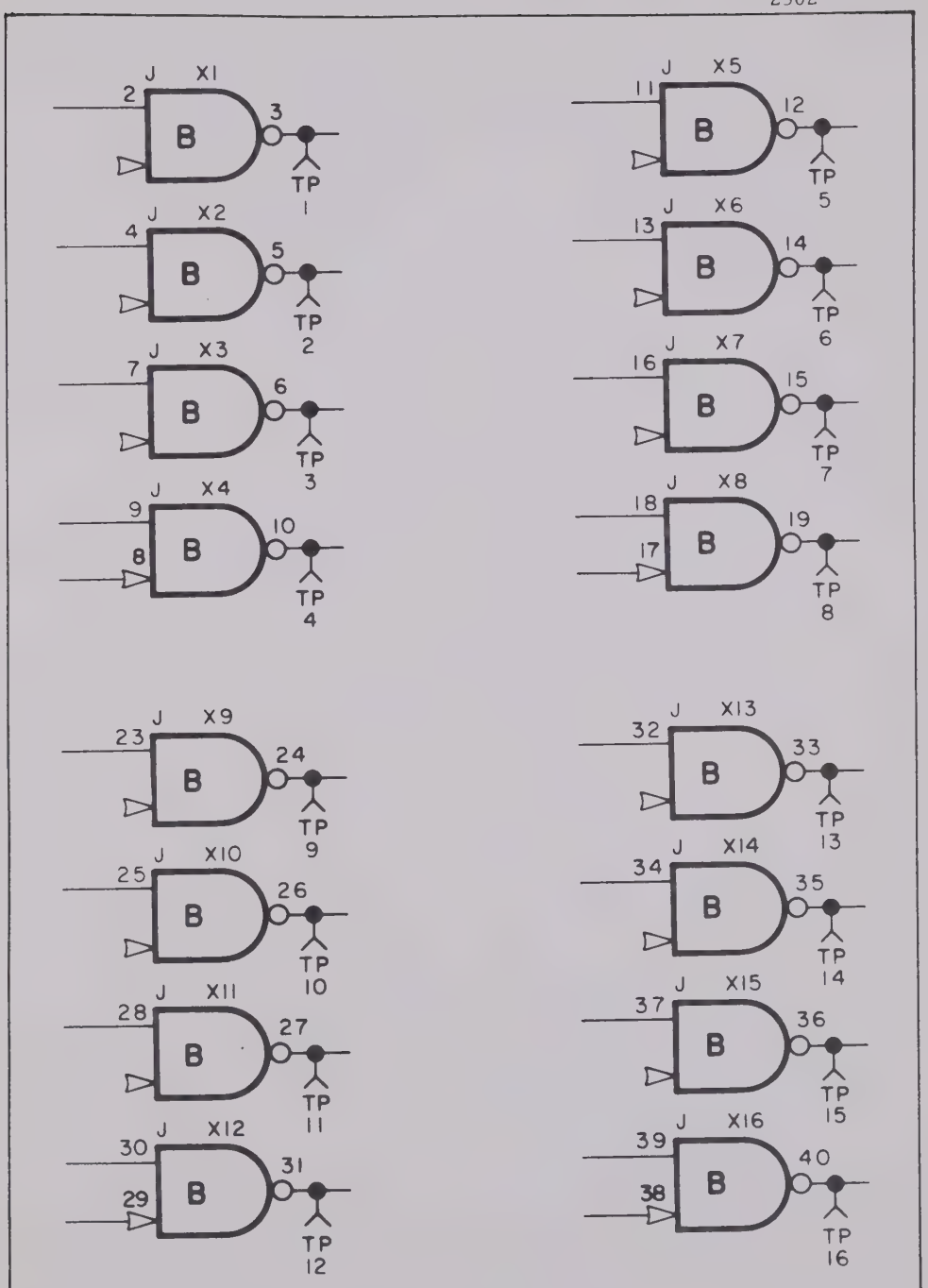


INTEGRATED CIRCUIT
PIN IDENTIFICATION
(TOP VIEW)



Card Layout Diagram

Figure 1 (Sheet 1 of 2)



Logic Symbols

Figure 1 (Sheet 2 of 2)

EMR MODEL 2503 12-2 INPUT NAND GATES
DIGITAL LOGIC CARD

1. DESCRIPTION

The EMR Model 2503 12-2 Input NAND Gates (12-2NA) Digital Logic Card contains three SG143 SUHL (Sylvania Universal High Level Logic) integrated circuit modules. Each SUHL module Z1, Z2, and Z3 contains four 2-input NAND Gates as shown in Figure 1. The 12-2NA Digital Logic Card is used in applications where individual 2-input NAND gates are required and where each NAND gate output must be capable of driving six standard loads*. Where a driving capability of up to 12 standard loads* per gate is required, the NAND gates on the identically-configured EMR Model 2504 12-2 Input NAND Buffer Gates (12-2NAB) Digital Logic Card are used. Additional applications of the 12-2NA Digital Logic Card are discussed in Paragraph 3.

2. SPECIFICATIONS

Overall Logic Card specifications are given in Paragraph 2.1 and detailed SUHL Module specifications are presented in Paragraph 2.2. Physical specifications are illustrated in Figure 1.

2.1 Logic Card Specifications

a. Number of Integrated Circuit Modules: 3.
b. Module Type: SG143 SUHL Integrated Circuit.
c. Module Circuit: Four 2-input NAND gates.
d. Total Number of Circuits: 12 NAND gates.
e. Number of Inputs: 24.
f. Number of Outputs: 12.
g. Output Polarity: Inverted.
h. Supply Voltage: +5.0 ±0.25V.
i. Supply Current: 48 Ma.
j. Operating Temperature: 0°C to 75°C.

2.2 SG143 SUHL Integrated Circuit Module Specifications

a. Input Specifications:

(1) Number: 8.
(2) Input Impedance: 1 standard load* per input.
(3) Maximum Input Voltage: +5.5V (logic ONE.)
(4) Input Levels:
Logic ONE = +3V (+1.9 to +5V)
Logic ZERO = 0V (0V to +1.1V)

b. Output Specifications:

(1) Number of Outputs: 4.
(2) Output Rise Time: 5 nanoseconds maximum per gate loaded with 6 standard loads* having a total capacitive load of 15 Pf.
(3) Output Fall Time: 8 nanoseconds maximum per gate when loaded with 6 standard loads* having a total capacitive load of 15 Pf.
(4) Average Propagation Delay: 20 nanoseconds maximum per gate when loaded with 6 standard loads* having a total capacitive load of 15 Pf.
(5) Drive Capability: Each gate can drive a maximum of 6 standard loads* having a total capacitive load of 600 Pf.
(6) Output Voltage Swing:
Logic ZERO: 0V to 0.45V.
Logic ONE: +3 to +5V.
(7) Short Circuit Protection: An output may be shorted to ground with no permanent degradation of the circuit.

3. LOGIC CIRCUIT APPLICATIONS

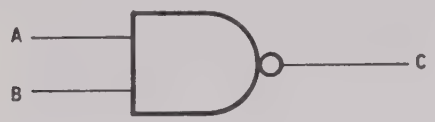
Typical applications for the NAND gate circuits on the EMR Model 2503 12-2 Input NAND Gates Digital Logic Card are discussed in the following paragraphs.

3.1 2-Input NAND Gates

The 2-Input NAND Gate shown in the following figure is used wherever a NAND gate is required having two independent inputs and where the NAND gate output must be capable of driving six standard loads. Each input to the 2-input NAND gate represents one standard load. The application of a logic ZERO level to either of the two inputs generates a logic ONE at the output. The simultaneous application of logic ONE

* A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.

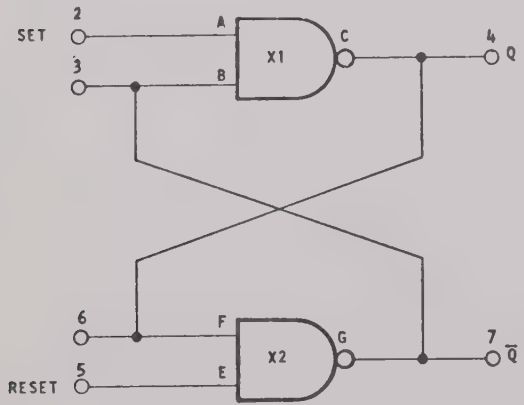
levels to the two inputs to the NAND gate generates a logic ZERO level at the output.

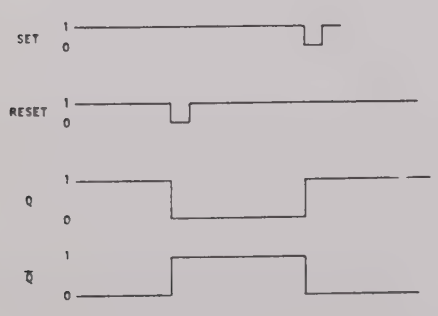


A	B	C
1	1	0
0	1	1
1	0	1
0	0	1

3.2 Flip-Flop Configuration

When two 2-input NAND gates on the 12-2NA Digital Logic Card are cross-coupled as shown in the following figure, a set-reset flip-flop is created.

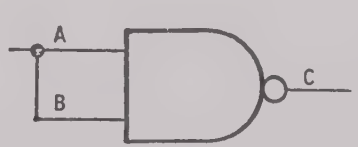




The set and reset inputs to the flip-flop are normally at the logic ONE level and the Q and $\overline{Q}$ outputs are normally at the ONE and ZERO levels respectively. A logic ZERO applied to either the set or reset input changes the state of the flip-flop. The accompanying timing diagram illustrates the operation of the flip-flop upon application of set and reset pulse inputs. The minimum width for the set or reset pulse input is 40 nanoseconds. The Q and $\overline{Q}$ outputs from the flip-flop are each capable of driving up to five standard loads. The flip-flop configuration shown is used where individual set-reset flip-flops are required and where each flip-flop output must be capable of driving up to five standard loads. Where a driving capability of up to 11 standard loads is required, the individual 2-input NAND gates on the EMR Model 2504 NAND Buffer Gates (12-2NAB) Digital Logic Card are used. In applications where simultaneous reset of several flip-flops is required, the simultaneously gated NAND gates on the EMR Model 2501 Digital Logic Cards are cross-coupled with the individual 2-input NAND gates on the EMR Model 2503 Digital Logic Cards to create the required number of flip-flop stores. Similarly, the NAND Buffer gates on the EMR Model 2502 and 2504 Digital Logic Cards may be cross-coupled to create a simultaneou sly reset flip-flop store having a driving capability of up to 11 standard loads per flip-flop output.

3.3 Inversion

When the two inputs to an individual NAND gate on the 12-2NA Digital Logic Card are externally connected together as shown in the following figure, the NAND gate functions as an inverter. The paralleled inputs still represent one standard load.



$AB = \overline{C}$

4. MAINTENANCE

Maintenance of the EMR Model 2503 12-2 Input NAND Gates Digital Logic Card is limited to the replacement of defective SG143 SUHL Integrated Circuit modules. A defective SG143 SUHL Integrated Circuit module is isolated using the EMR Model 2798Card Test Set and the test procedure outlined in Table 1.

CAUTION

Use minimum heat required to simultaneously loosen the module pins. Excessive heat will lift land area on card.

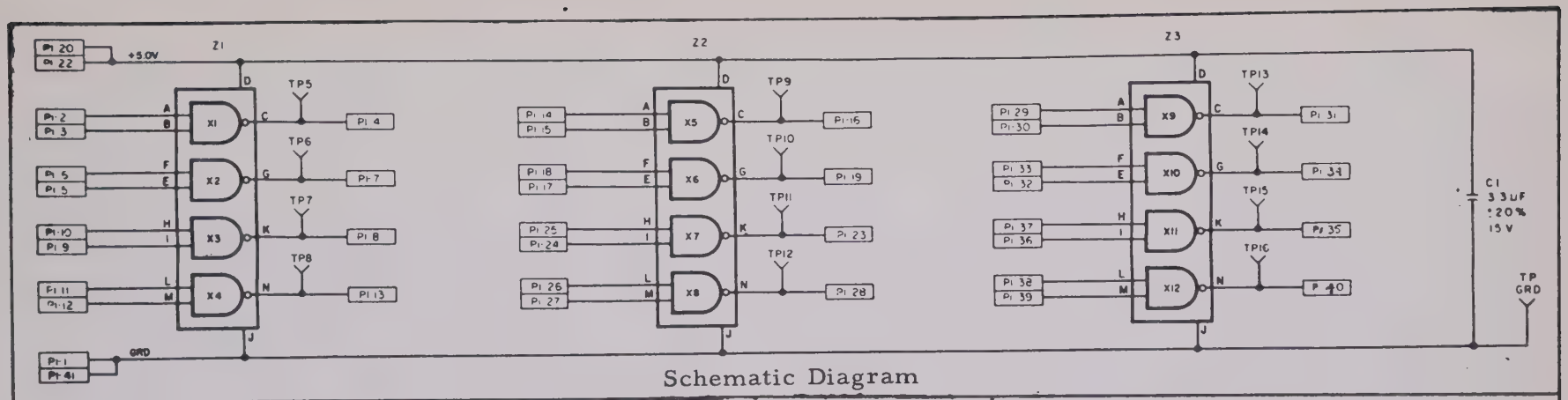
When the defective module has been isolated, the module is removed by simultaneously heating the 14 module contacts on land side of card and withdrawing module from opposite side of card.

The black dot on the replacement module is aligned with the corresponding plated dot on the printed-circuit card and the module is inserted into the card. The module contacts are soldered to the plated-through holes on the card using minimum heat and solder.

Table 1. EMR Model 2503 12-2 Input NAND Gates Digital Logic Card Test Procedure

NOTE

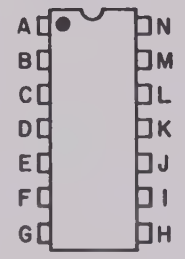
Card test procedure provided when EMR Model 2798 Card Test Set is ordered.



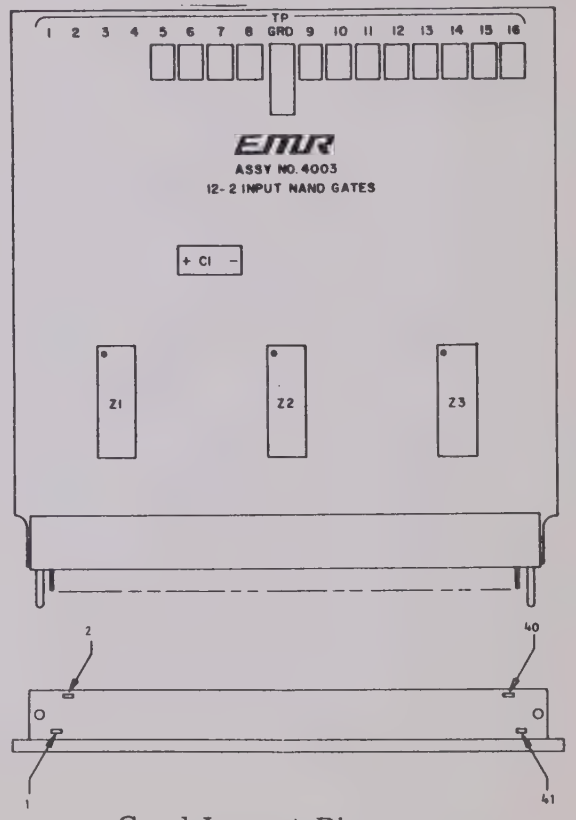
Schematic Diagram

CIRCUIT SYMBOL NO	DESCRIPTION	MANUFACTURER NAME	MANUFACTURER PART NO
	12-2 INPUT NAND GATES PRINTED-WIRING BOARD	EMR	204-99-00003
C1	CAPACITOR, 3.3 µF ±20%, 15V	EMR	336-21-33003
TP GRD	TEST JACK (BLACK)	AUGAT	8041-1G6
TP5 THRU TP16	TEST JACK (BLACK)	AUGAT	8046-1G6
Z1 THRU Z3	INTEGRATED CIRCUIT	SYLVANIA	SG143-03 SUHL

Parts List

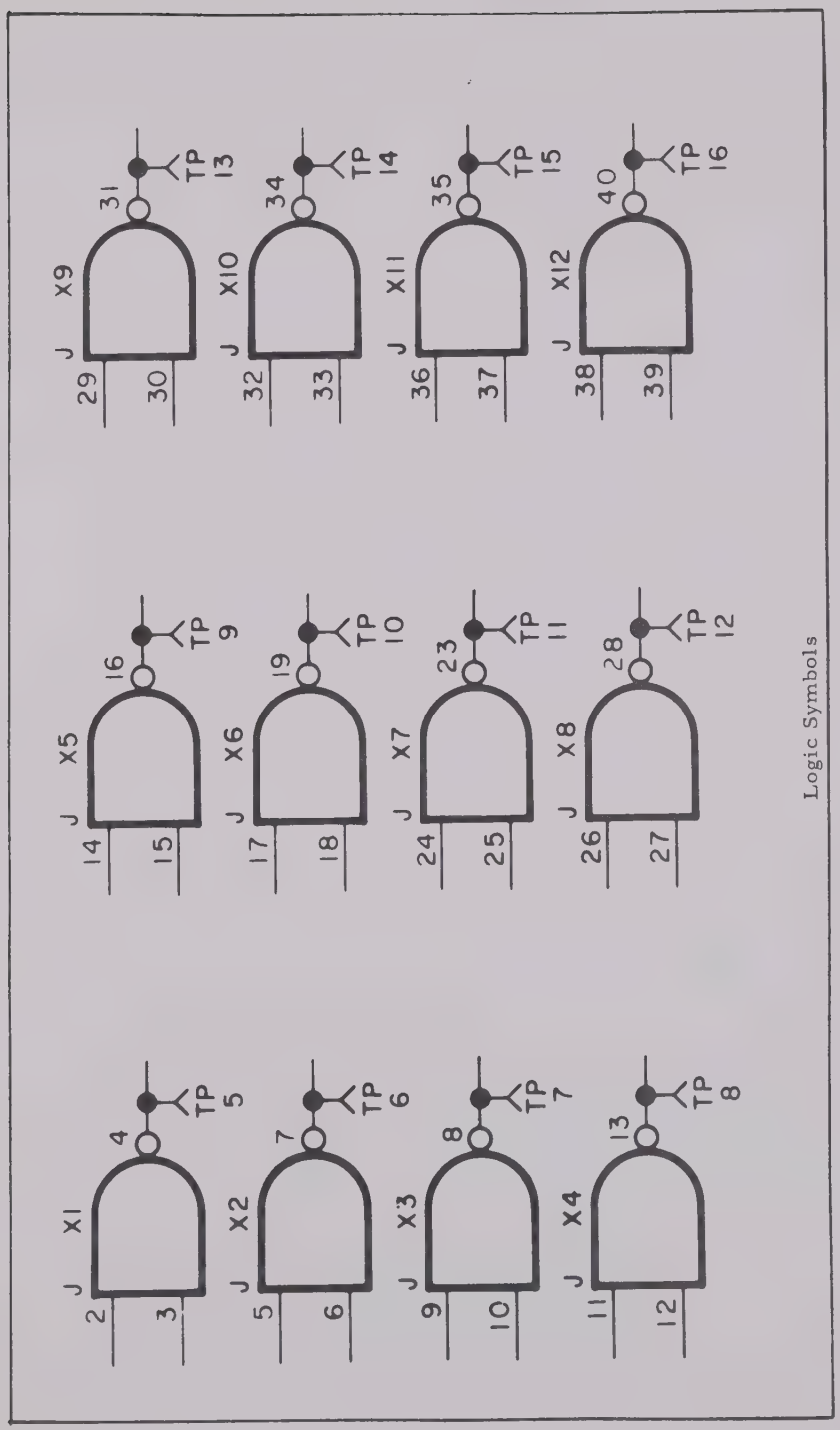


INTEGRATED CIRCUIT
PIN IDENTIFICATION
(TOP VIEW)



Card Layout Diagram

Figure 1 (Sheet 1 of 2)



Logic Symbols

Figure 1 (Sheet 2 of 2)

EMR MODEL 2506
FOUR 8-INPUT NAND GATES DIGITAL LOGIC CARD

1. DESCRIPTION

The EMR Model 2506 Four 8-Input NAND Gates (4-8NA) Digital Logic Card contains four SG63 SUHL (Sylvania Universal High-Level Logic) integrated-circuit modules. Each SUHL module Z1, Z2, Z3, and Z4 contains a single 8-input NAND as shown in Figure 1. The EMR Model 2506 4-8NA is used in applications requiring a NAND gate having eight independent inputs. Additional applications of the EMR Model 2506 4-8NA Digital Logic Card are discussed in paragraph 3.

2. SPECIFICATIONS

Overall Logic Card specifications are given in paragraph 2.1 and detailed SUHL Module specifications are presented in paragraph 2.2. Physical specifications are illustrated in Figure 1.

2.1 Logic Card Specifications

a. Number of Integrated-Circuit Modules: 4.
b. Module Type: SG63.
c. Module Circuit: 8-Input NAND Gate.
d. Number of Logic Inputs: 32.
e. Number of Outputs: 4.
f. Output Polarity: Inverted.
g. Supply Voltage: +5.0 ±0.25V.
h. Supply Current: 16 Ma.
i. Operating Temperature Range: 0 to +75°C.

2.2 SG63 SUHL Integrated-Circuit Module Specifications

a. Input Specifications:

1. Logic Inputs--8.
2. Input Impedance--One standard load* per input.
3. Maximum Input Voltage--+5.5V (logic ONE).
4. Input Levels--

(a) Logic ONE: +3V (+1.9V to +5V).
(b) Logic ZERO: 0V (0V to +1.1V).

b. Output Specifications:

1. Number of Outputs--1.
2. Output Rise Time--5 nanoseconds maximum when loaded with six standard loads* having a total capacitive load of 15 Pf.
3. Output Fall Time--8 nanoseconds maximum when loaded with six standard loads* having a total capacitive load of 15 Pf.
4. Average Propagation Delay--20 nanoseconds maximum when loaded with six standard loads* having a total capacitive load of 15 Pf.
5. Drive Capability--A maximum of six standard loads* can be driven having a total capacitive load of 600 Pf.
6. Output Voltage Swing--

(a) Logic ONE: +3V to +5V.
(b) Logic ZERO: 0V to 0.45V.

7. Short-Circuit Protection--An output may be shorted to ground with no permanent degradation of the circuit.

3. LOGIC CIRCUIT APPLICATIONS

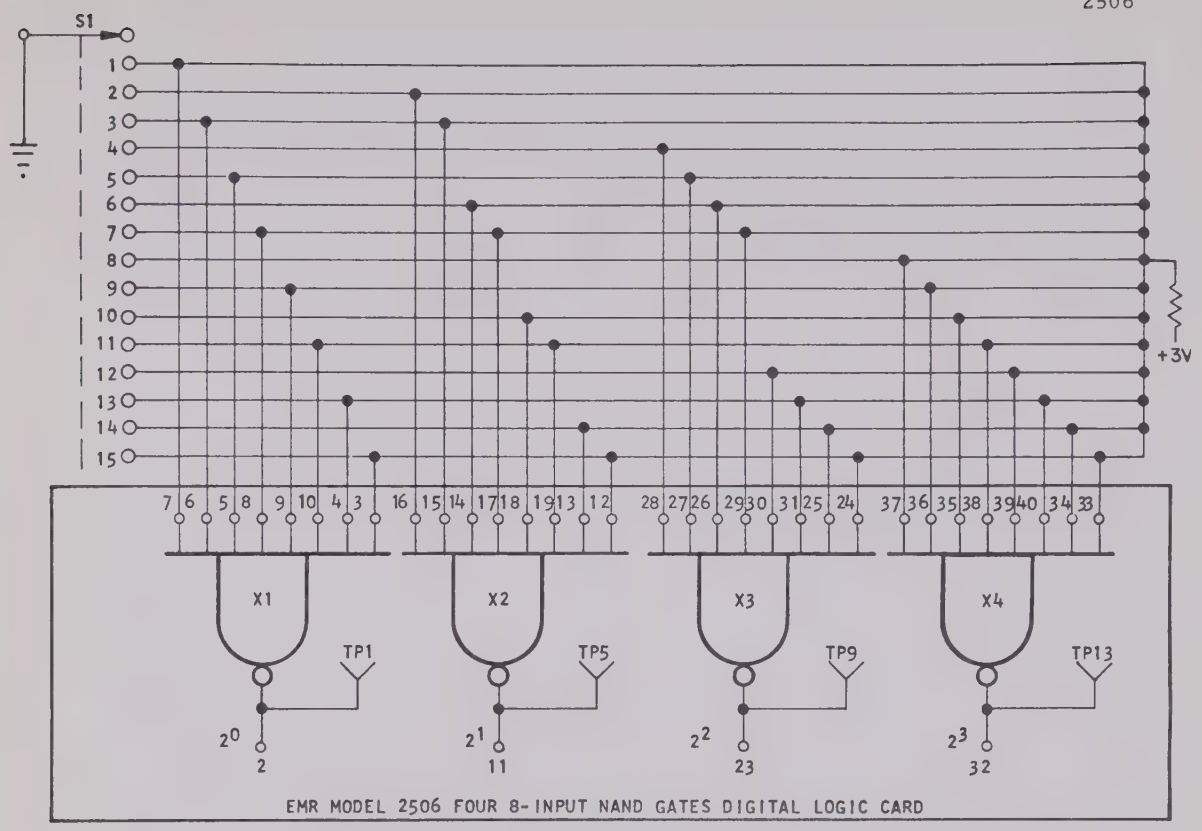
A typical application for the circuits included on the EMR Model 2506 4-8NA Digital Logic Card is described in the following paragraph.

3.1 Decimal-to-Binary Encoder Gates

The four 8-input NAND gates on the EMR Model 2506 4-8NA Digital Logic Card may be connected to switch S1 as shown in the following figure to encode each switch position into a four-bit binary number.

When switch S1 is in position 0, the inputs to the four NAND gates are all at +3-volt (logic ONE) level and the four NAND gate outputs are at the zero-volt (logic ZERO) level. When switch S1 is set to position 1, the switch applies a logic ZERO to NAND gate X1 and the NAND-gate output

*A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.



switches to the logic ONE level. The four parallel NAND-gate outputs now represent the binary equivalent of decimal 1 (1000). In each switch position, switch S1 applies a logic ZERO level to the appropriate NAND gates to generate the logic ONE levels in the binary-encoded equivalent of the switch position.

4. MAINTENANCE

Maintenance of the EMR Model 2506 Four 8-Input NAND Gates Digital Logic Card is limited to the replacement of defective SG63 SUHL Integrated-Circuit Modules. A defective SG63 SUHL Integrated-Circuit Module is isolated using the EMR Model 2798 Card Test Set and the procedures outlined in Table 1.

CAUTION

Use minimum heat required to simultaneously loosen the module pins. Excessive heat will lift the land area on the card.

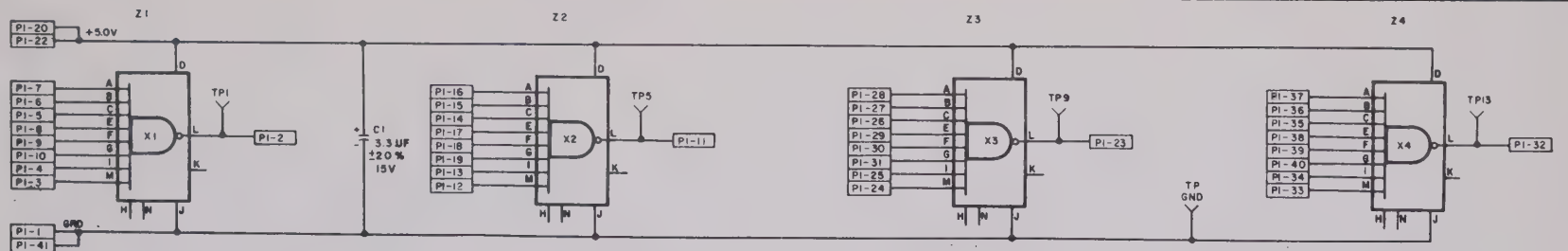
When a defective module has been isolated, the module is removed by simultaneously heating the 14 contacts on the land side of the card and withdrawing the module from the opposite side of the card.

The black dot on the replacement module is aligned with the corresponding plated dot on the printed-circuit card and the module is inserted into the card. The module contacts are soldered to the plated-through holes on the card using minimum heat and solder.

Table 1. EMR Model 2506 Four 8-Input NAND Gates Digital Logic Card Test Procedure

NOTE

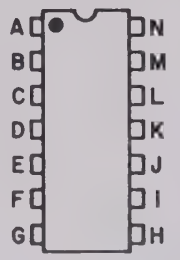
Card test procedure provided when EMR Model 2798 card test set is ordered.



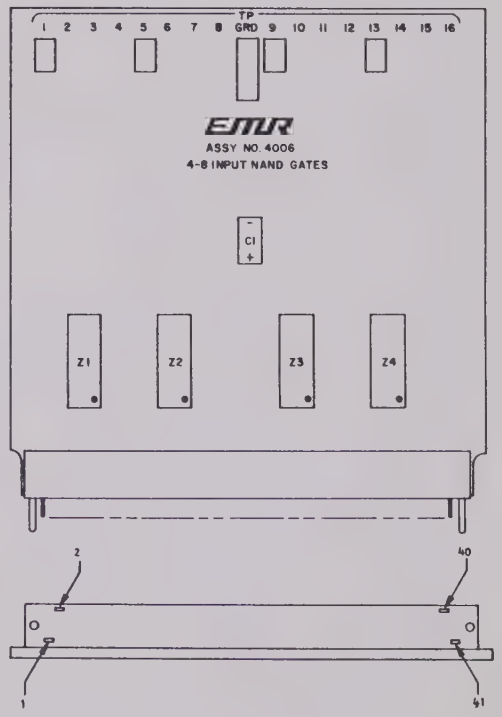
Schematic Diagram

CIRCUIT SYMBOL NO.	DESCRIPTION	MANUFACTURER NAME	MANUFACTURER PART NO.
	FOUR 8-INPUT NAND GATES PRINTED-WIRING BOARD	EMR	204-99-00006
C1	CAPACITOR, 3.3 µF ±20%, 15V	EMR	336-21-33003
TP GRD	TEST JACK (BLACK)	AUGAT	8041-1G6
TP1, 5, 9, AND 13	TEST JACK (BLACK)	AUGAT	8046-1G6
Z1 THRU Z4	INTEGRATED CIRCUIT	SYLVANIA	SG63-03 SUHL

Parts List



INTEGRATED CIRCUIT
PIN IDENTIFICATION
(TOP VIEW)



Card Layout Diagram

Figure 1 (Sheet 1 of 2)

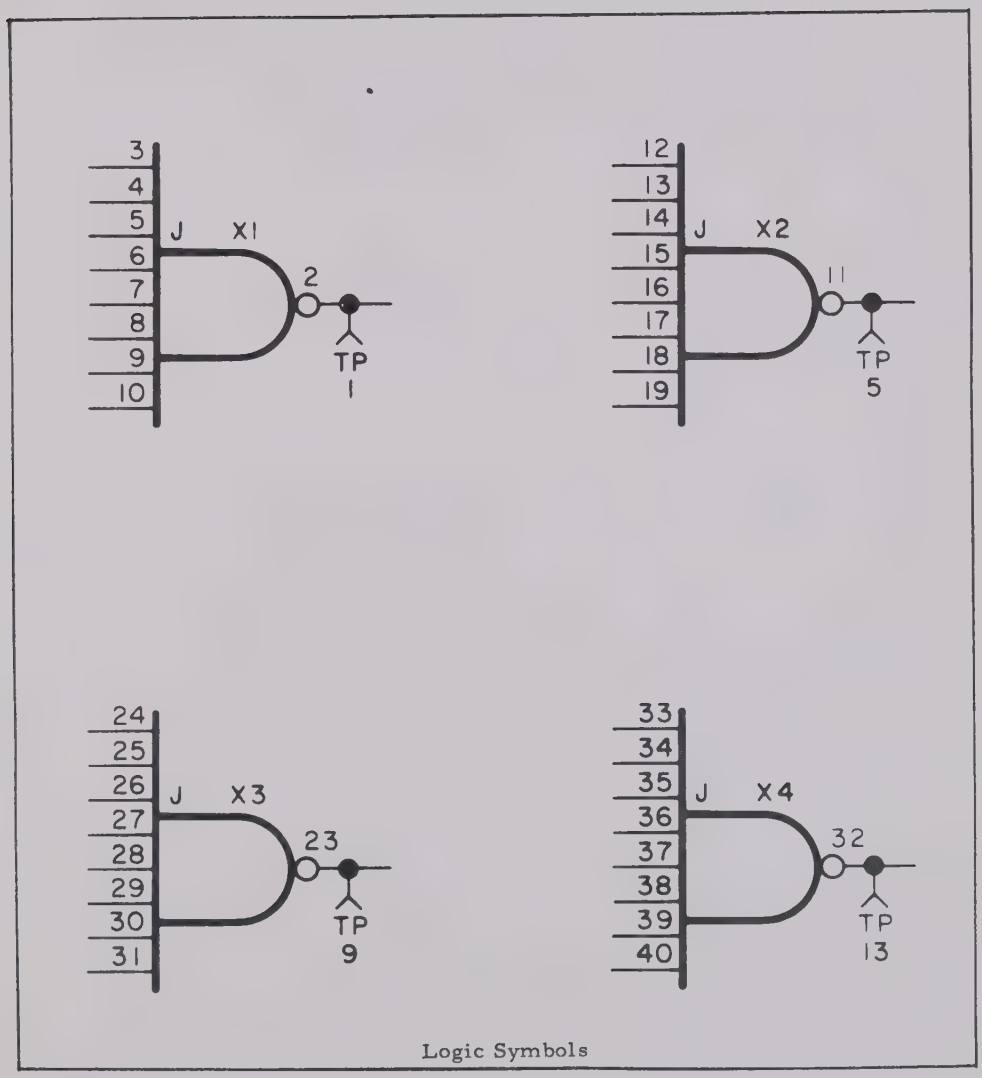


Figure 1 (Sheet 2 of 2)

EMR MODEL 2546
TWO 4-BIT STORAGE REGISTERS DIGITAL LOGIC CARD

1. DESCRIPTION

The EMR Model 2546 Two 4-Bit Storage Registers (2-4STR) Digital Logic Card contains 7 SG143 SUHL (Sylvania Universal High Level Logic) Integrated-Circuit Modules connected as shown in Figure 1 to create two independent 4-bit storage registers. Each SG143 Integrated-Circuit Module contains four 2-input NAND gate circuits. Each four-bit storage register has two set inputs, two reset inputs, and four data-assertion inputs. Each storage register provides assertion and negation outputs for each of the four stored data bits. The applications of the four-bit storage register circuits on the EMR Model 2546 2-4STR Digital Logic Card are discussed in paragraph 3.

2. SPECIFICATIONS

Overall logic card specifications are given in paragraph 2.1 and detailed circuit specifications are presented in paragraph 2.2. Physical specifications are illustrated in Figure 1.

2.1 Logic Card Specifications

a. Number of Modules: 7.
b. Module Type: SG143.
c. Module Circuit: Four 2-Input NAND Gates.
d. Number of Inputs: 18 (9 inputs for each 4-bit storage register).
e. Number of Outputs: 18 (four assertion and four negation outputs from each storage register plus an S1-S2 output from each storage register for use as a master system reset).
f. Supply Voltage: +5.0 ±0.25V.
g. Supply Current: 112 Ma.

2.2 Detailed Circuit Specifications (X1 or X2)

a. Circuit Function: Four-bit storage register.
b. Module Type: SG143.
c. Module Circuit: Four 2-Input NAND Gates.
d. Modules per Circuit: 3.5.
e. Input Specifications:

1. Number of Inputs--

(a) Set Inputs: 2.
(b) Reset Inputs: 2.
(c) Data Inputs: 4.
(d) Clock Input: 1.

2. Input Impedance--

(a) Set Inputs: One standard load* per input.
(b) Reset Inputs: One standard load* per input.
(c) Data Inputs: One standard load* per input.
(d) Clock Input: Four standard loads.*

3. Input Levels--

(a) Logic ONE: +3V (+1.9V to +5V).
(b) Logic ZERO: 0V (0V to +1.1V).

4. Maximum Input Voltage-- +5.5V (logic ONE).

5. Input Signal Characteristics--

(a) Reset Pulse: A logic ONE level at inputs R1 and R2 or a logic ZERO level at $\overline{C}$ input for a minimum of 20 nanoseconds.
(b) Set Pulse: Logic ZERO level at S1 or S2 for a minimum of 20 nanoseconds.
(c) Data Inputs: Data must be stable for the same time period as the set pulse width but delayed 20 nanoseconds.

f. Output Specifications:

1. Number of Outputs--9 (Q and $\overline{Q}$ outputs, four flip-flops, plus S1-S2 output for use as a master system reset).
2. Output Rise Time (Q and $\overline{Q}$ Outputs)--5 nanoseconds maximum when loaded with five standard loads* having a total capacitive load of 15 Pf.
3. Output Fall Time (Q and $\overline{Q}$ Outputs)--8 nanoseconds maximum when loaded with five standard loads* having a total capacitive load of 15 Pf.
4. Average Propagation Delay (Q and $\overline{Q}$ Outputs)--Data will be stable on the assertion (Q) output not later than 60 nanoseconds after the leading (negative-going) edge of the set pulse input. Data will be stable on the negation ($\overline{Q}$) output not later than 80 nanoseconds after the leading edge of the set pulse input.

*A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.

5. Drive Capability (Q and $\overline{Q}$ Outputs)--The Q and $\overline{Q}$ sides of each flip-flop are each capable of driving up to five standard loads* having a total capacitive load of 600 Pf.
6. Drive Capability ($\overline{C}$ Output)--The $\overline{C}$ output is capable of driving two standard loads* having a total capacitive load of 15 Pf.
7. Output Voltage Swing--

   (a) Logic ZERO: 0V to 0.45V.
   (b) Logic ONE: +3V to +5V.

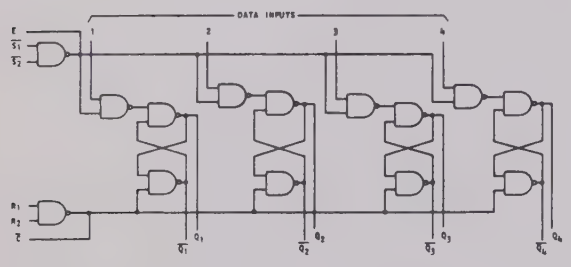
8. Short Circuit Protection--An output may be shorted to ground with no permanent degradation of the circuit.

3. LOGIC CIRCUIT APPLICATIONS

The applications of the 4-bit storage register circuits on the EMR Model 2546 Digital Logic Card are discussed in the following paragraphs.

3.1 Four-Bit Storage Register

Each four-bit storage register consists of 14 2-input NAND gates connected as shown in the following figure.



The set and reset lines control register reset and data entry. Prior to data entry, the register must be reset to clear the logic ONEs previously stored in the register. This is necessary because the single-sided data input lines enter only logical ONEs into the register. The register is reset when either the R1 and R2 inputs are high or when the $\overline{C}$ input is low. If register reset is to be accomplished from a single control line, the R1 and R2 inputs are tied together. Data is entered when $\overline{S1}$ or $\overline{S2}$ is low. Any logical ONEs present on the data input lines are set into the respective storage stages when the $\overline{S1}$ and $\overline{S2}$ inputs are both low.

Register reset operation can be controlled from one of several control inputs, depending on the method of control line interconnection. Two methods of register reset control are as follows:

a. Reset Selection Control--When the E output is connected to the R1 and R2 inputs as a master system reset, only the register or registers having set inputs are selected for reset and data entry. When this method of interconnection is used, the set input pulse must be of a longer duration than the master reset to assure that data is properly entered.

b. $\overline{C}$ Reset Control--The $\overline{C}$ output can be grounded through an external switch to reset the register. The $\overline{C}$ output can also be used as an extension of the reset signal for control of external circuits. When so used, the $\overline{C}$ output is capable of driving up to two standard loads.

3.2 Extended Storage Register

Register length can be extended by connecting the respective register control lines in parallel with the driving sources. Up to six 4-bit storage registers may be connected in parallel for register lengths of up to 24 bits. When so used, the control-line configuration for each register must be wired identically. For example, when a single control line is used, the $\overline{C}$ output from each register must be connected to its respective $\overline{S1}$ input.

4. MAINTENANCE

Maintenance of the EMR Model 2546 Two 4-Bit Storage Registers Digital Logic Card is limited to the replacement of defective SG143 SUHL Integrated-Circuit Modules. A defective SG143 SUHL Integrated-Circuit Module is isolated using the EMR Model 2798 Card Test Set and the test procedures outlined in Table 1.

CAUTION

Use minimum heat required to simultaneously loosen the module pins. Excessive heat will lift the land areas on the card.

When the defective module has been isolated, the module is removed by simultaneously heating the 14 pins on the land side of the card and

*A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.

withdrawing the module from the opposite side of the card.

The black dot on the replacement module is aligned with the corresponding plated dot on the printed-circuit card and the module is inserted into the card. The module contacts are soldered to the plated-through holes on the card using minimum heat and solder.

Table 1. EMR Model 2546 Two 4-Bit Storage Registers Digital Logic Card Test Procedure

NOTE

Card test procedure provided when EMR Model 2798 Card Test Set is ordered.

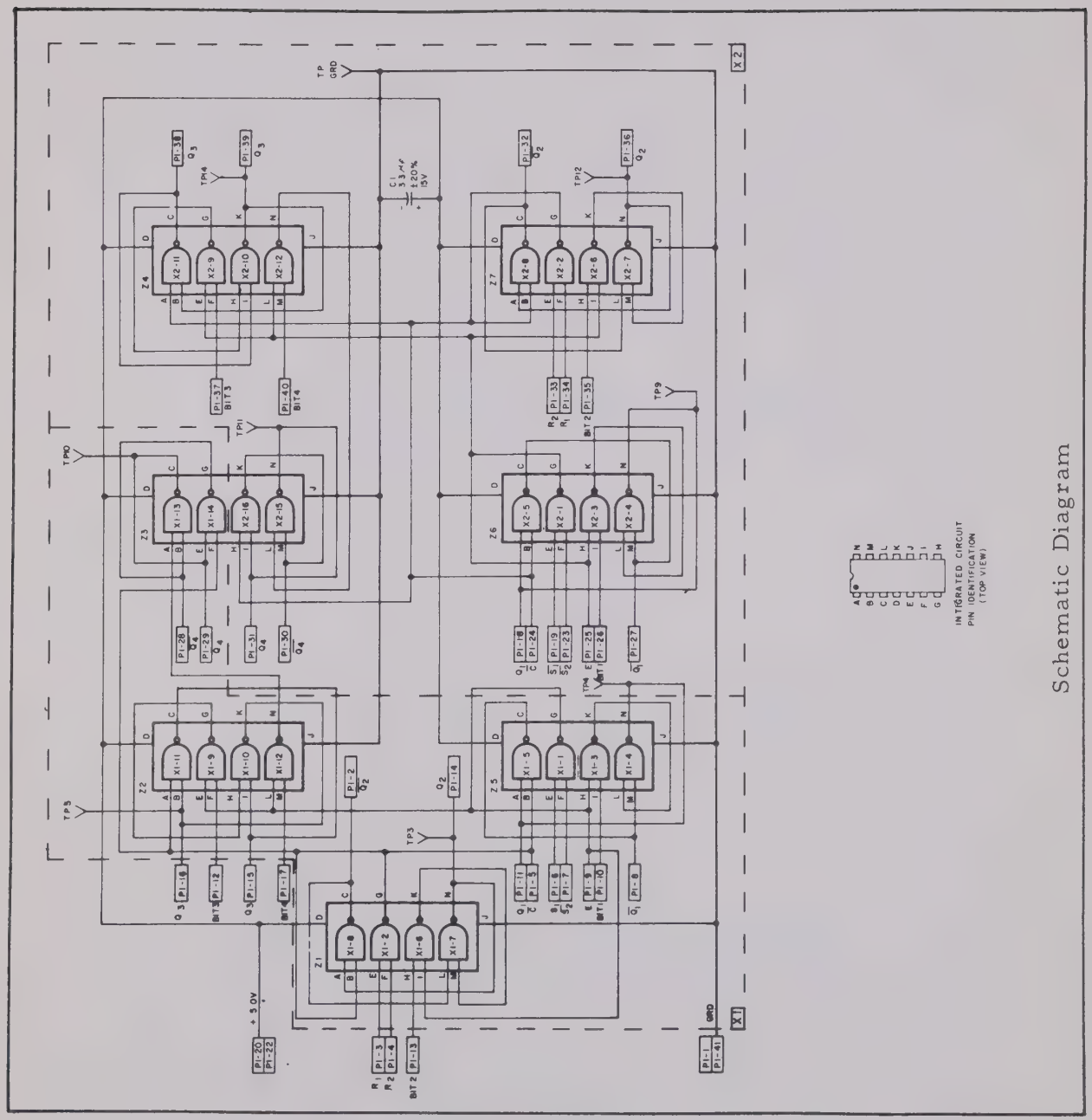


Figure 1 (Sheet 1 of 3)

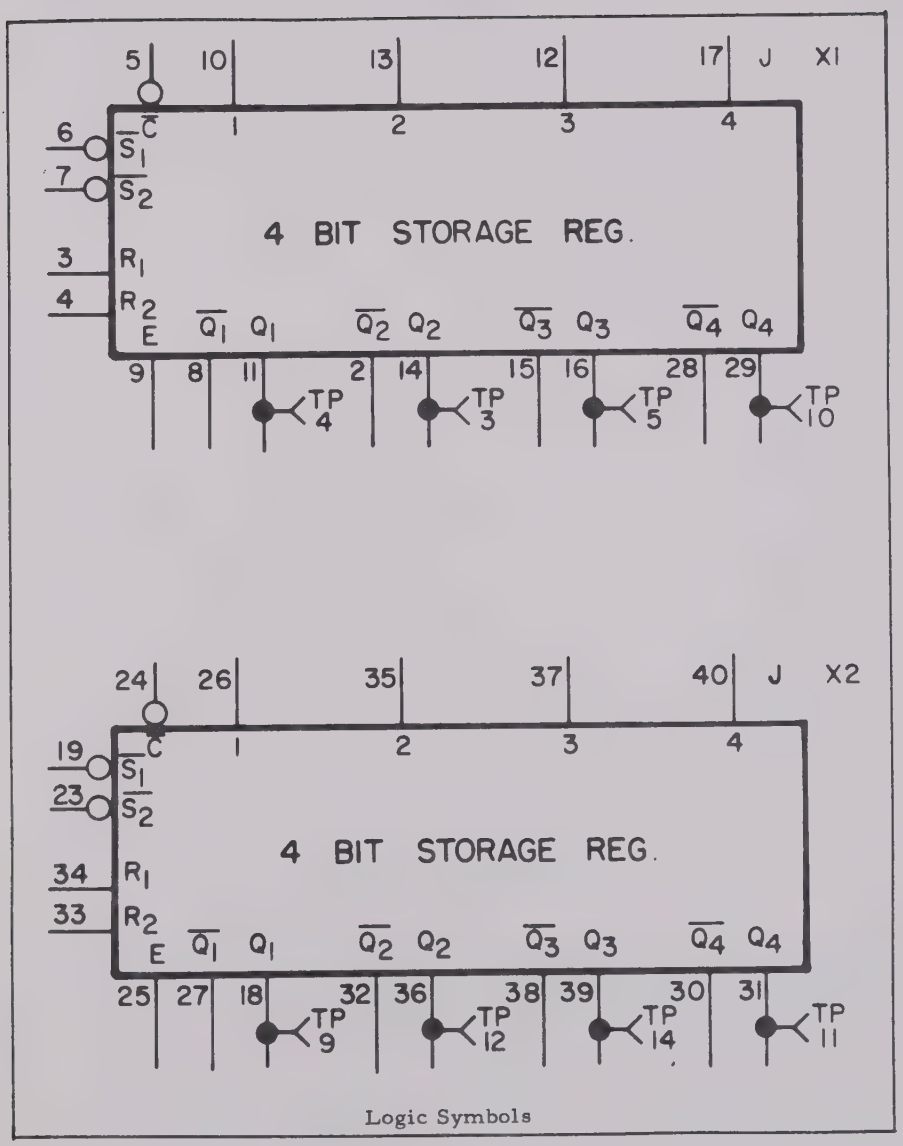
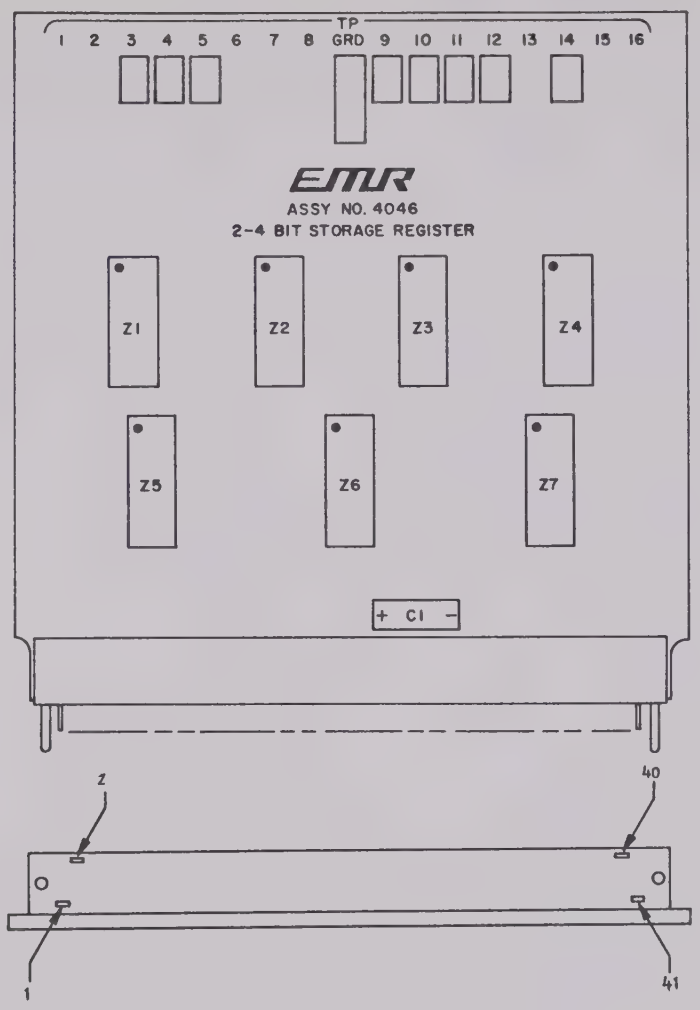


Figure 1 (Sheet 2 of 3)



Card Layout Diagram

CIRCUIT SYMBOL NO.	DESCRIPTION	MANUFACTURER	
		NAME	PART NO.
	TWO 4-BIT STORAGE REGISTERS PRINTED-CIRCUIT BOARD	EMR	204-99-00048
C1	CAPACITOR, 3.3 μF ±20%, 15V	EMR	336-21-33003
TP GRD	TEST JACK (BLACK)	AUGAT	8041-1G6
TP 3, 4, 5, 9, 10, 11, 12, AND 14	TEST JACK (BLACK)	AUGAT	8046-1G6
Z1 THRU Z7	INTEGRATED CIRCUIT	SYLVANIA	SG143-03 SUHL

Parts List

Figure 1 (Sheet 3 of 3)

EMR MODEL 2564
FOUR GATED ONE SHOTS DIGITAL LOGIC CARD

1. DESCRIPTION

The EMR Model 2564 Four Gated One Shots (4GOS) Digital Logic Card shown in Figure 1 contains four variable-pulse-width gated one-shot multivibrators and four fixed-pulse-width (40 nanoseconds) one-shot multivibrators. The variable and fixed-pulse-width one-shot multivibrator circuits shown are comprised of a combination of SUHL (Sylvania Universal High-Level Logic) Integrated-Circuit Modules and discrete components. Each of the four fixed-pulse-width multivibrator circuits is comprised of an SG142 (four 2-input NAND buffer gates) SUHL Integrated-Circuit Module and two 100 Pf capacitors. Each of the four gated variable-pulse-width one-shot multivibrator circuits consists of an SG92 (exclusive OR with complement) SUHL Integrated-Circuit Module, a single NPN transistor, three resistors, and a capacitor selected by the customer. The value of the capacitor selected by the customer determines the width of the pulse generated by the one-shot multivibrator. A formula for computing the correct capacitor for a desired pulse width is provided in paragraph 3.

2. SPECIFICATIONS

Overall Logic Card specifications are given in paragraph 2.1 and detailed circuit specifications are presented in paragraph 2.2. Physical specifications are illustrated in Figure 1.

2.1 Logic Card Specifications

a. Number of Modules: 8.
b. Module Types:

1. SG142--Four 2-input NAND buffer gates.
2. SG92--Exclusive OR with complement.

c. Number of Circuits: 8.

1. 4 Fixed-Pulse-Width (40 nanoseconds) One-Shot Multivibrator Circuits.
2. 4 Gated Variable-Pulse-Width One-Shot Multivibrator Circuits.

d. Number of Inputs: 4.

1. One input to each of four fixed-pulse-width one-shot multivibrator circuits.
2. Five inputs to each of four gated variable-pulse-width one-shot multivibrator circuits.

e. Number of Outputs: 12.

1. Two outputs from each of four fixed-pulse-width one-shot multivibrator circuits.
2. One output from each of four gated variable-pulse-width one-shot multivibrator circuits.

f. Output Polarity:

1. Separate assertion and negation outputs from each fixed-pulse-width one-shot multivibrator circuit.
2. Assertion output from each gated variable-pulse-width one-shot multivibrator circuit.

g. Supply Voltage: +5.0 V ±0.25V.
h. Supply Current: 57 Ma.
i. Operating Temperature: 0°C to +75°C.

2.2 Detailed Circuit Specifications

a. Fixed-Pulse-Width One-Shot Multivibrator Circuit (X1, X2, X3, or X4):

1. Input Specifications--

(a) Number of Inputs: 1.
(b) Input Impedance: Two standard loads.*
(c) Maximum Input Voltage: +5.5V (logic ONE).
(d) Input Polarity: Positive-going (logic ZERO-to-ONE level) pulse. Trigger occurs on positive-going edge of pulse.
(e) Input Levels: Logic ONE, +3V (+1.9V to +5V); logic ZERO, 0V (0V to +1.1V).

2. Output Specifications--

(a) Number of Outputs: 2.
(b) Output Pulse Width: 40 nanoseconds.
(c) Drive Capability:

Assertion Output--12 standard loads* each--C_T = 600 Pf.
Negation Output--10 standard loads* each--C_T = 600 Pf.

*A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.

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(d) Output Rise Time: 5 nanoseconds maximum at each output into rated maximum number of standard loads.* C_T = 15 Pf.
(e) Output Fall Time: 8 nanoseconds maximum at each output into rated maximum number of standard loads.* C_T = 15 Pf.
(f) Maximum Propagation Delay Time:

Assertion Output--40 nanoseconds maximum.
Negation Output--20 nanoseconds maximum.

(g) Output Voltage Swing:

Logic ONE-- +3V to +5V.
Logic ZERO--0V to 0.45V.

(h) Short-Circuit Protection: An output may be shorted to ground with no permanent degradation of the circuit.

b. Gated Variable-Pulse-Width One-Shot Multivibrator Circuit (X5, X6, X7, or X8):

1. Input Specifications--

(a) Number of Inputs: 5.

Input AND Gate--3.
Output NAND Gate--2.

(b) Input Impedance: One standard load* per input.
(c) Maximum Input Voltage: +5.5V (logic ONE).
(d) Input Polarity: Positive-going (logic ZERO-to-ONE level) pulses. Triggering occurs when inputs A, B, and C are all positive. When inputs M and N are both positive, the one-shot output is gated to the output.
(e) Input Levels: Logic

Logic ONE-- +3V (+1.9V to +5V).
Logic ZERO--0V (0V to +1.1V).

2. Output Specifications--

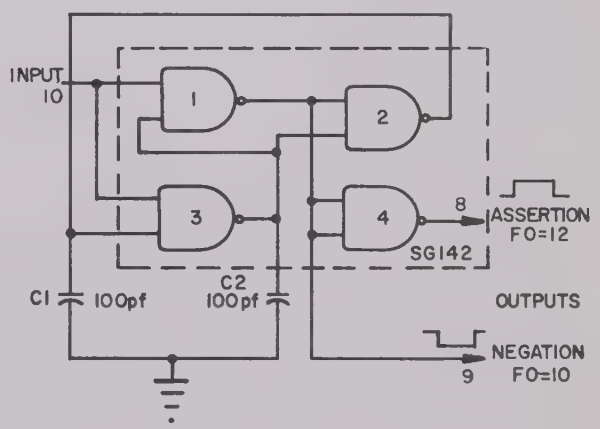
(a) Number of Outputs: 1.
(b) Output Pulse Width: Variable (see paragraph 3.)
(c) Output Polarity: Positive-going (logic ZERO-to-ONE level pulses).
(d) Drive Capability: 12 standard loads* C_T = 600 Pf.
(e) Output Rise Time: 5 nanoseconds maximum into rated maximum number of standard loads* C_T = 15 Pf.
(f) Output Fall Time: 8 nanoseconds maximum into rated maximum number of standard loads* C_T = 15 Pf.
(g) Average Propagation Delay Time: 42 nanoseconds maximum into rated maximum number of standard loads* C_T = 15 Pf.

3. THEORY OF OPERATION

The operation of the fixed pulse width and gated variable pulse width one-shot multivibrator circuits is described in the following paragraphs.

3.1 Fixed-Pulse-Width One-Shot Multivibrator Circuit (X1, X2, X3, or X4)

The fixed-pulse-width one-shot multivibrator circuit shown in the following figure is comprised of an SG142 (four 2-input NAND buffer gates) SUHL Integrated-Circuit Module and two 100-Pf capacitors.



When the input at pin 10 is low, NAND gates 1 and 3 outputs are at a logic ONE level of +3V. The logic ONE level at the output of NAND gate 3 maintains a charge of +3V on capacitor C2. The logic ONE level at the output of NAND gate 1

* A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.

maintains NAND gate 2 in conduction and capacitor C1 is discharged to ground through the conducting NAND gate.

When the input at pin 10 rises toward a logic ONE level, NAND gate 1 conducts applying a logic ZERO level to the negation output at pin 9 and to the inputs to NAND gates 2 and 4. The output of NAND gate 4 applies a logic ONE level to the assertion output at pin 8.

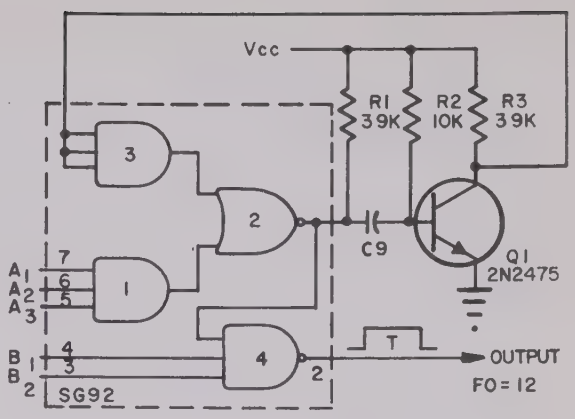
The logic ZERO level from NAND gate 1 cuts off NAND gate 2 and a logic ONE level is applied to capacitor C1 and to the input to NAND gate 3. After 20 nanoseconds, capacitor C1 has charged to a sufficient level to turn on NAND gate 3 and discharge capacitor C2 toward ground. Twenty nanoseconds after NAND gate 3 turns on, capacitor C2 has discharged to a level sufficient to cut off NAND gate 1. When NAND gate 1 cuts off, a logic ONE level is simultaneously applied to the negation output at pin 9 and to the inputs to NAND gates 2 and 4. NAND gate 4 inverts the logic ONE input and applies a logic ZERO level to assertion output pin 8. The capacitor C1 charge time and capacitor C2 charge time produces a 40-nanosecond pulse at the one-shot assertion and negation outputs. Since the logic ZERO output from NAND gate 3 has already cut off NAND gate 2, the logic ONE output from NAND gate 1 has no effect on NAND gate 2 nor the charge on capacitor C9.

When the input at pin 10 drops to a logic ZERO level, the assertion and negation outputs from the one shot do not change levels since NAND gate 1 is being held at cutoff by the logic ZERO level output from NAND gate 3. The logic ONE-to-ZERO transition at input pin 10 cuts off NAND gate 3 and capacitor C2 starts to charge. Twenty nanoseconds after NAND gate 3 cuts off, the charge on capacitor C2 has risen sufficiently to turn on NAND gate 2 and discharge capacitor C1 to ground. NAND gate 2 remains turned on and NAND gate 3 remains cut off until the next positive-going input to the one-shot multivibrator.

3.2 Gated Variable-Pulse-Width One-Shot Multivibrator Circuit (X5, X6, X7, or X8)

The gated variable-pulse-width one-shot multivibrator circuit shown in the following figure is comprised of an SG92 (exclusive OR with complement) SUHL Integrated-Circuit Module, a single NPN transistor, three resistors, and a capacitor selected by the customer.

The width of the one-shot pulse output is determined by the discharge time of customer-supplied capacitor C9 through 10K ohm resistor R2. The one-shot multivibrator is in the quiescent state



when any one of the inputs to AND gate 1 is low. In this condition, capacitor C9 is charged plus to minus through resistors R1 and R2, respectively. The negative charge on the R2 connection of capacitor C9 is not sufficient to cut off transistor Q1 and a logic ZERO level is applied to AND gate 3. The logic ZERO level input to AND gate 3 maintains the AND gate in conduction and a logic ZERO level is maintained at the second input to NOR gate 2. With both inputs to NOR gate 2 at a logic ZERO level, the NOR gate is cut off and a positive charge is maintained on capacitor C9 through resistor R1 at the NOR gate output.

When all inputs to AND gate 1 are high, the AND gate cuts off and a logic ONE level is applied to NOR gate 2. The logic ONE level input to NOR gate 2 turns on the NOR gate and capacitor C9 discharges through the NOR gate to ground. The negative transition at the output of NOR gate 2 is simultaneously applied to NAND gate 4 and coupled through capacitor C9 to the base of transistor Q1. If the remaining two inputs to NAND gate 4 are high, the negative-going transition of the NOR gate 2 output is inverted by NAND gate 4 and applied to the one-shot output as the positive-going edge of the one-shot pulse.

When the negative-going transition at the NOR gate 2 output has occurred, the R2 end of capacitor C9 became positive and the capacitor charged through the low impedance emitter-to-base junction of transistor Q1. The electron current flow from ground through the emitter-to-base junction to the positive side of capacitor C9 back biases the emitter-to-base junction and the transistor cuts off. When transistor Q1 cuts off, a logic ONE level is applied to the input to AND gate 3. The logic ONE level input to AND gate 3 cuts off the AND gate and a logic ONE level is applied to one NOR gate 2 input.

When an input to AND gate 1 goes low, AND gate 1 turns on and a logic ZERO level is applied to NOR gate 2. This input to NOR gate 2 has no effect on the NOR gate since the output from NAND gate 3 is being held at a logic ONE level by transistor Q1. NOR gate 2 remains on and the one-shot output remains high until the output transistor Q1 turns on and the output from NAND gate 3 goes to a ZERO logic level.

When transistor Q1 cuts off, capacitor C9 discharges through 10K ohm resistor R2 until the charge has decreased sufficiently to forward bias the emitter-to-base junction of transistor Q1 and the transistor turns on. When transistor Q1 turns on, a logic ZERO level is applied to AND gate 3 and the gate turns on applying a logic ZERO level to NOR gate 2. With both inputs to NOR gate 2 at a logic ZERO level, the NOR gate cuts off and capacitor C9 charges almost instantaneously through the cascade output of NOR gate 2 to a logic ONE level of +3.5V. At that time, the cascade output of NAND gate 2 starts to turn off, requiring the current through R1 to charge the capacitor fully to +5V. The short charge time for capacitor C9 is due to the low output impedance of NOR gate 2.

When the output from NOR gate 2 rises to a logic ONE level of +3V, NAND gate 4 turns on and the one-shot output drops to a logic ZERO level. The one-shot output remains at a logic ZERO level until all inputs to NAND gate 1 are again at a logic ONE level. Two of the three inputs to NAND gate 4 can be used to gate the one-shot pulse to the output. When these two inputs are tied to a logic ONE source, the entire one-shot pulse is gated to the output.

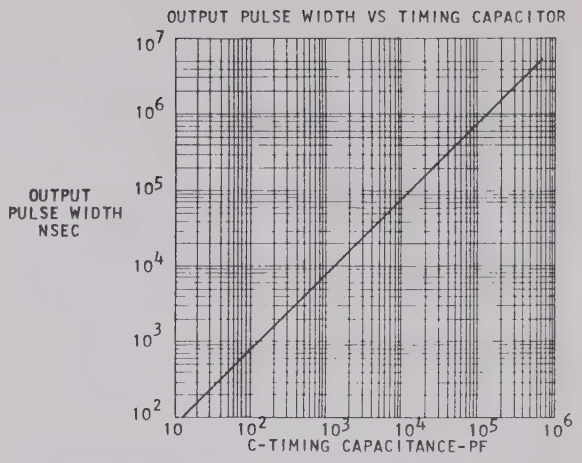
It can be seen from the previous discussion that the width of the one-shot pulse depends on the discharge time of customer-supplied capacitor C9 through 10K ohm resistor R2. The technician servicing the card may compute the pulse width associated with a particular timing capacitor on the card by using the following formula or by referring to the accompanying pulse-width-vs-timing capacitor chart.

t = 0.72 RC nanoseconds, where:
t = required pulse width in nanoseconds
K = 10 (in kilohms)
C = required external capacitance in Pf

t = 7.2C.

4. APPLICATIONS

The applications for the fixed-pulse-width one-shot multivibrator circuits and the gated variable-pulse-width one-shot multivibrator circuits are described in the following paragraphs.



GATED ONE-SHOT M.V. CIRCUIT C-VS-t CHART

4.1 Fixed-Pulse-Width One-Shot Multivibrator Circuits

a. The fixed-pulse-width one-shot multivibrator (FOS) circuit may be used in applications where a fixed 40-nanosecond pulse is required.

b. The fixed-pulse-width one-shot multivibrator is used to shape the trigger pulse input to a gated variable-pulse-width one-shot multivibrator (GOS) when the input trigger pulse width exceeds the width of the GOS pulse output. The positive-going FOS output is connected to the GOS input.

4.2 Gated Variable-Pulse-Width One-Shot Multivibrator Circuits

a. The gated variable-pulse-width one-shot multivibrator circuit is used in applications where a one-shot pulse width greater than 40 nanoseconds is required. Total one-shot pulse width is obtained when the two gating inputs are tied to a logic ONE source.

b. The gated variable-pulse-width one-shot multivibrator circuit can also be used as an inhibit gate. When dynamic signals are applied to the two gating inputs, the signals are blanked for the period of the one-shot pulse.

NOTE

A fixed-pulse-width one-shot multivibrator circuit must precede a gated variable-pulse-width one-shot multivibrator circuit when the width of the trigger pulse input to the GOS exceeds the width of the GOS output. The positive-going FOS output is connected to the GOS input.

5. MAINTENANCE

Maintenance of the EMR Model 2564 Four Gated One Shots Digital Logic Card is limited to the replacement of defective SG142 and SG92 SUHL Integrated-Circuit Modules or the discrete components associated with these modules. A defective FOS or GOS circuit is isolated using the EMR Model 2798 Card Test Set and the test procedures outlined in Table 1.

CAUTION

Use minimum heat required to loosen modules or discrete components. Excessive heat will lift the land areas on card.

When a defective module has been found to be the cause of the malfunction, the module is removed by simultaneously heating the 14 module contacts on the land side of the card and withdrawing the module from the opposite side of the card.

The black dot on the replacement module is aligned with the corresponding plated dot on the printed-circuit card and the module is inserted into the card. The module contacts are soldered to the plated-through holes on the card using minimum heat and solder. Observe keying when replacing transistors and observe polarity when replacing capacitors.

Table 1. EMR Model 2564 Four Gated One Shots Digital Logic Card Test Procedure

NOTE

Card test procedure provided when EMR Model 2798 Card Test Set is ordered.

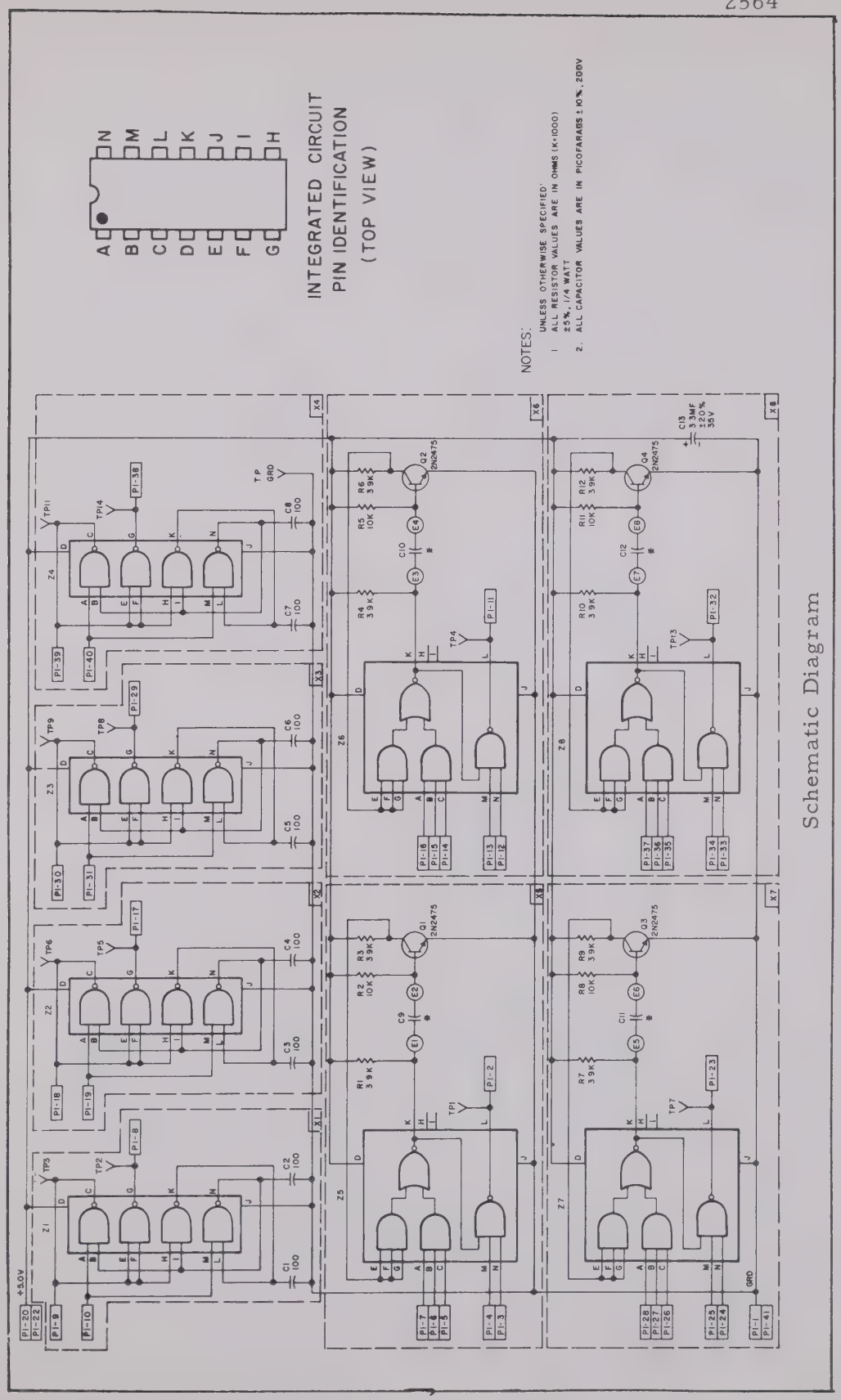


Figure 1 (Sheet 1 of 3)

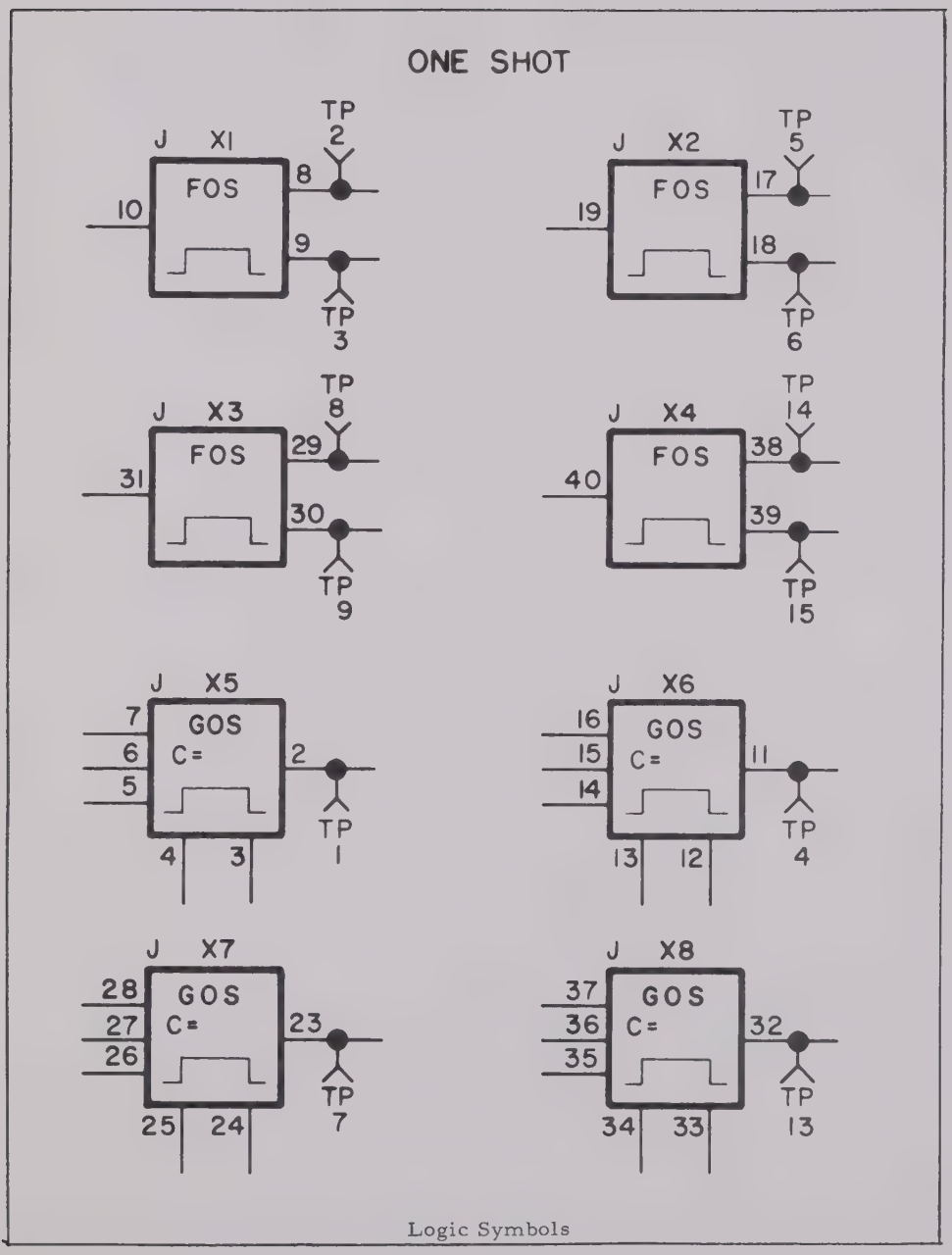


Figure 1 (Sheet 2 of 3)

EMR MODEL 2567
ONE 8-TO-10 BIT SHIFT REGISTER/B DIGITAL LOGIC CARD

1. DESCRIPTION

The EMR Model 2567 One 8-to-10 Bit Shift Register/B (1-8/10SRB) Digital Logic Card, shown in Figure 1, contains one 8-bit shift register with buffered clock and reset control lines and two independent single-input JK flip-flops. The 8-bit shift register is comprised of eight SF52 and one SG142 SUHL (Sylvania Universal High Level Logic) Integrated-Circuit Modules. Each SF52 SUHL module contains a single JK flip-flop. The SG142 SUHL module contains four 2-input NAND buffer gates. The four NAND buffer gates are externally connected as shown to form two parallel pairs. The two pairs of paralleled NAND gates invert and buffer the clock and reset inputs to the 8-bit shift register. The NAND gate clock and reset outputs are also applied to the card connector pins where they may be used to drive the two independent JK flip-flops on the card or to drive additional external circuits. The applications of the circuits on the EMR Model 2567 8-to-10 Bit Shift Register/B Digital Logic Card are discussed in paragraph 3.

2. SPECIFICATIONS

Overall Logic Card Specifications are given in paragraph 2.1 and Detailed Circuit Specifications are presented in paragraph 2.2. Physical specifications are illustrated in Figure 1.

2.1 Logic Card Specifications

a. Number of Modules: 11.
b. Module Types: SF52, JK Flip-Flop; SG142, Four 2-Input NAND Buffer Gates.
c. Number of Circuits: 3.

1. One 8-Bit Shift Register
2. Two Single-Input JK Flip-Flops

d. Number of Inputs: 14.

1. 8-Bit Shift Register X1--4.
2. JK Flip-Flop X2--5.
3. JK Flip-Flop X3--5.

e. Number of Outputs: 8.

1. Buffered Clock--1.
2. Buffered Reset--1.
3. 8-Bit Shift Register X1--2.
4. JK Flip-Flop X1--2.
5. JK Flip-Flop X2--2.

f. Output Polarity:

1. Buffered Clock Pulse--Positive-going logic ZERO-to-ONE level.
2. Buffered Reset Pulse--Positive-going logic ZERO-to-ONE level.
3. 8-Bit Shift Register X1--Separate assertion and negation outputs.
4. JK Flip-Flop X2--Separate assertion and negation outputs.
5. JK Flip-Flop X3--Separate assertion and negation outputs.

g. Supply Voltage: +5.0 ±0.25V.
h. Supply Current: 136 Ma.
i. Operating Temperature: 0°C to +75°C.

2.2 Detailed Circuit Specifications

a. One 8-Bit Shift Register Circuit X1

1. Input Specifications:

(a) Number of Inputs--4.

Clock Pulse
Reset Pulse
J Input
K Input

(b) Input Impedance--

Clock Pulse: Two standard loads*
Reset Pulse: Two standard loads*
J Input: One standard load*
K Input: One standard load*

(c) Input Pulse Width--

Clock Pulse: 20 nanoseconds minimum
Reset Pulse: 40 nanoseconds minimum

(d) Input Pulse Polarity--

Clock Pulse: Negative going (data on J and K inputs must be stable when clock is low, data is entered on positive-going clock-pulse edge).

*A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.

Reset Pulse: Positive going (the shift register is reset when reset pulse goes high).

(e) Maximum Positive-Going Clock Pulse Slope--200 nanoseconds.
(f) Maximum Input Voltage--+5.5V (logic ONE).
(g) Input Levels--

Logic ONE: +3V (+1.9V to +5V)
Logic ZERO: 0V (0V to +1.1V)

(h) Reset Time--120 nanoseconds minimum after last positive-going clock pulse edge.

2. Output Specifications:

(a) Number of Outputs--2 (Q and $\overline{Q}$)
(b) Output Rise Time--5 nanoseconds maximum when loaded with one standard load* having a total capacitive load of 15 Pf.
(c) Output Fall Time--8 nanoseconds maximum when loaded with one standard load* having a total capacitive load of 15 Pf.
(d) Maximum Propagation Delay Times--

To turn ON side OFF: 20 nanoseconds when loaded with one standard load* having a total capacitive load of 15 Pf.
To turn OFF side ON: 40 nanoseconds when loaded with one standard load* having a total capacitive load of 15 Pf.

(e) Drive Capability--Q and $\overline{Q}$ outputs for bits 1 through 7 are capable of driving up to 11 standard loads* having a total capacitive load of 600 Pf. Bit 8 is capable of driving up to 12 standard loads.*

(f) Output Voltage Swing--

Logic ONE: +3V to +5V
Logic ZERO: 0V to 0.45V

(g) Short-Circuit Protection--An output may be shorted to ground with no permanent degradation of the circuit.

b. Single-Input JK Flip-Flop X2 or X3

1. Input Specifications:

(a) Number of Inputs--5.

Clock Pulse
Set Input
Reset Input
J Input
K Input

(b) Input Impedance--

Clock Pulse: 1.5 standard loads*
Other Inputs: One standard load* each

(c) Input Pulse Width--

Clock Pulse: 20 nanoseconds minimum
Set Pulse: 40 nanoseconds minimum
Reset Pulse: 40 nanoseconds minimum

(d) Input Pulse Polarity--

Clock Pulse: Positive going (data entered on negative-going clock pulse edge)
Set Pulse: Negative going
Reset Pulse: Negative going

(e) Maximum Negative-Going Clock Pulse Slope--200 nanoseconds
(f) Maximum Input Voltage-- +5.5V (logic ONE)
(g) Input Levels--

Logic ONE: +3V (+1.9V to +5V)
Logic ZERO: 0V (0V to +1.1V)

(h) Set or Reset Time--120 nanoseconds minimum after negative clock pulse transition.

2. Output Specifications:

(a) Number of Outputs--2 (Q and $\overline{Q}$)
(b) Output Rise Time--5 nanoseconds maximum when loaded with one standard load* having a total capacitive load of 15 Pf.

* A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.

(c) Output Fall Time--8 nanoseconds maximum when loaded with one standard load* having a total capacitive load of 15 Pf.

(d) Maximum Propagation Delay Times--

To turn ON side OFF: 20 nanoseconds when loaded with one standard load* having a total capacitive load of 15 Pf.
To turn OFF side ON: 40 nanoseconds when loaded with one standard load* having a total capacitive load of 15 Pf.

(e) Drive Capability--Q and $\overline{Q}$ outputs are each capable of driving up to 12 standard loads* having a total capacitive load of 600 Pf.

(f) Output Voltage Swing--

Logic ONE: +3V to +5V
Logic ZERO: 0V to 0.45V

(g) Short-Circuit Protection--An output may be shorted to ground with no permanent degradation of the circuit.

3. APPLICATIONS

Typical applications for the 8-bit shift register/B and two independent single-input JK flip-flop circuits on the EMR Model 2567 One 8-to-10 Bit Shift Register/B Digital Logic Card are described in the following paragraphs.

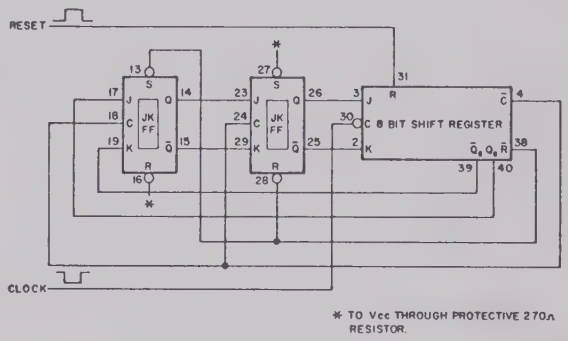
3.1 Shift Register

The basic 8-bit shift register/B, shown in Figure 1, is most useful as a serial-to-parallel converter. The two independent single-input JK flip-flop circuits on the card provide for the expansion of the shift register to ten bits without the need for adding external components. When using the single-input JK flip-flops for expanding the register length, the buffered clock and reset output lines can be tied directly to the JK flip-flop clock and reset (or set) lines.

The register can be expanded up to 16 bits in length with external JK flip-flops connected to this card with no external clock or reset buffering. Several of these cards can be connected in tandem to obtain larger register lengths. When doing this, the clock and reset inputs to each card are paralleled while observing input and output loading ratings of the driving source. When paralleling the clock and reset drive inputs, the maximum clock frequency limits are reduced because of the added capacitive loading from each paralleled gate.

3.2 Decimal Ring Counter

The 8-bit shift register and two independent single-input JK flip-flops on the EMR Model 2567 One 8-to-10 Bit Shift Register/B Digital Logic Card can be connected as shown in the following figure to create a decimal ring counter. With the connections shown, the reset command sets a logic ONE in stage 1 and logic ZEROs in the nine remaining stages.



All output bits (Q1 through Q10) and their complements are available on the connector pins for use as required. The logic ONE in stage 1 is shifted right by the clock pulses followed by ZEROs (stage 10--Q_8 and $\overline{Q_8}$ enter logic ZEROs into stage 1) until the logic ONE appears in stage 10, and is then reinserted into stage 1 on the next clock pulse. This type of counter is useful for applications requiring decimal decoding. Only one of the ten stages will contain a logic ONE during a given clock interval. Whenever the logic ONE appears in a preselected position, it is used to activate another logic sequence, such as reset, etc. Higher scale stages can be added to this register to extend the scale of the counter if required. To do this, the last bit of this counter ($\overline{Q_8}$) is connected to the clock input of the next decade. Each decade counts the number of clock pulse transitions in decades as the logic ONE is circulated around each decade.

4. MAINTENANCE

Maintenance of the EMR Model 2567 One 8-to-10 Bit Shift Register/B Digital Logic Card is limited

*A standard load is defined as that impedance which will allow 0.1 Ma leakage current to flow for a logic ONE level of +4.5V and 1.66 Ma load current to flow for a logic ZERO level of 0V.

to the replacement of defective SF52 and SG142 SUHL Integrated-Circuit Modules. A defective SF52 or SG142 Integrated-Circuit Module is isolated using the EMR Model 2798 Card Test Set and the test procedures outlined in Table 1.

CAUTION

Use minimum heat required to simultaneously loosen the module pins. Excessive heat will lift the land areas on the card.

When the defective module has been isolated, the module is removed by simultaneously heating the 14 module contacts on the land side of the card and withdrawing the module from the opposite side of the card.

The black dot on the replacement module is aligned with the corresponding plated dot on the printed-circuit card and the module is inserted into the card. The module contacts are soldered to the plated-through holes on the card using minimum heat and solder.

Table 1. One 8-to-10 Bit Shift Register/B Digital Logic Card Test Procedure

NOTE

Card test procedure provided when EMR Model 2798 Card Test Set is ordered.

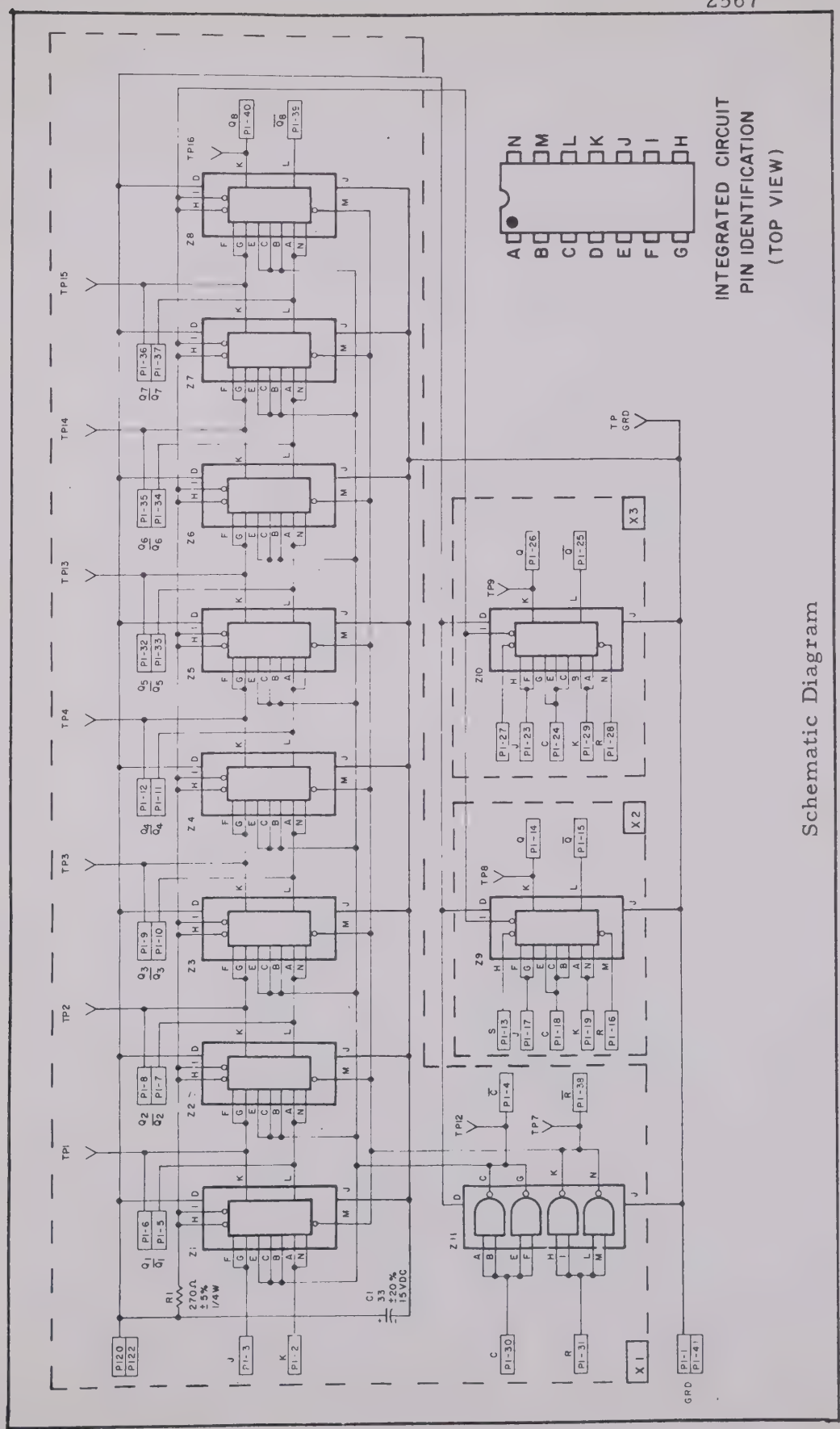


Figure 1 (Sheet 1 of 3)

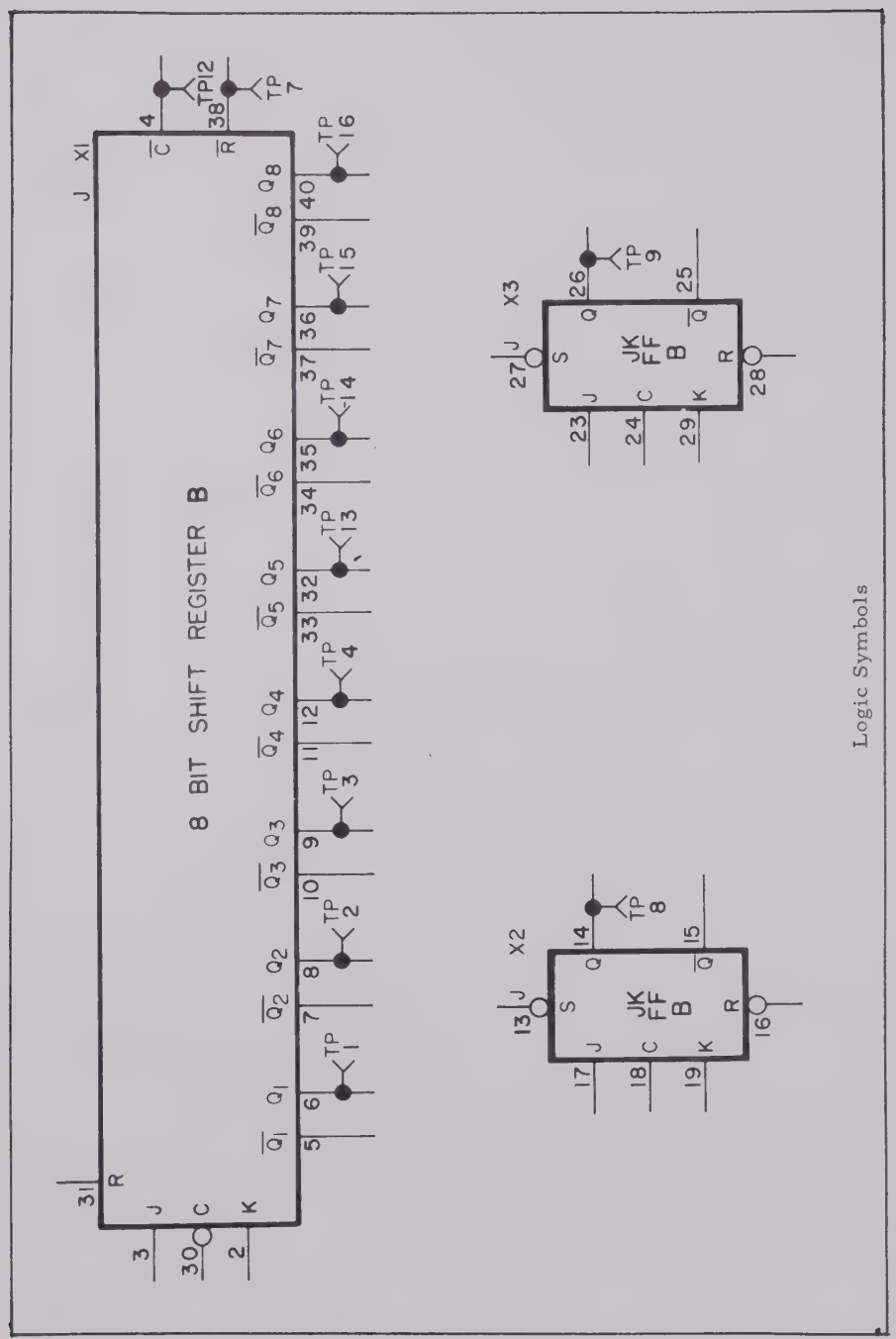
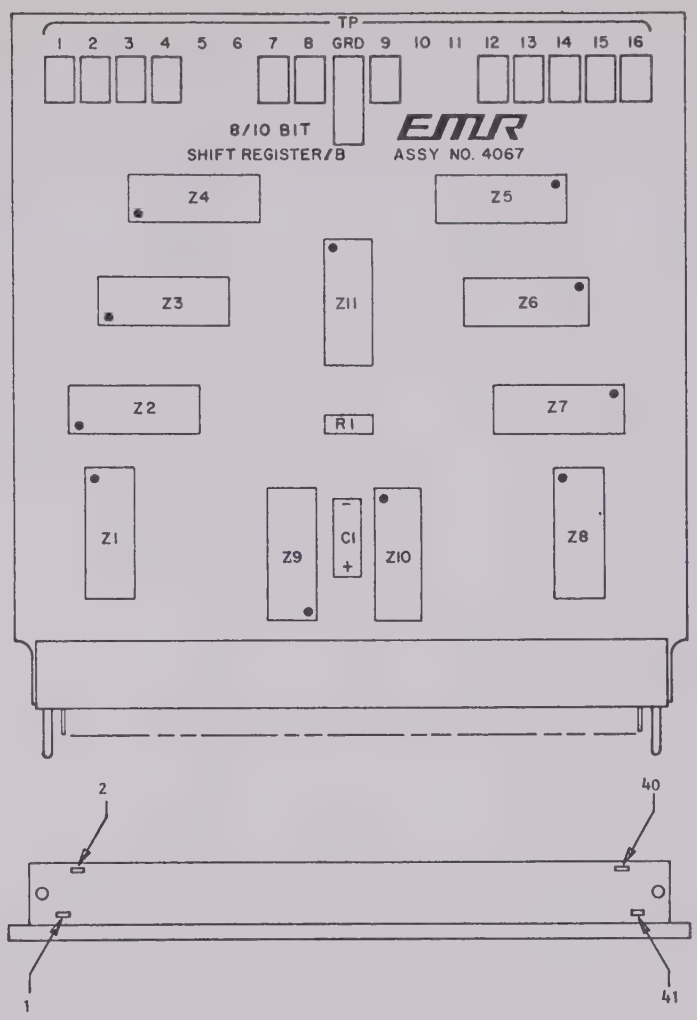


Figure 1 (Sheet 2 of 3)



Card Layout Diagram

CIRCUIT SYMBOL NO.	DESCRIPTION	MANUFACTURER	
		NAME	PART NO.
	ONE 8 TO 10 BIT SHIFT REGISTER/B PRINTED-WIRING BOARD	EMR	204-99-00051
C1	CAPACITOR, 3.3 µF ±20%, 15V	EMR	336-21-33003
R1	RESISTOR, 270 OHM ±5%, 1/4W	MIL-R-11/8	RC07GF271J
TP GRD	TEST JACK (BLACK)	AUGAT	8041-1G6
TP1, 2, 3, 4, 7, 8, 9, AND 12 THRU TP16	TEST JACK (BLACK)	AUGAT	8046-1G6
Z1 THRU Z10	INTEGRATED CIRCUIT	SYLVANIA	SF52-03 SUHL
Z11	INTEGRATED CIRCUIT	SYLVANIA	SG142-03 SUHL

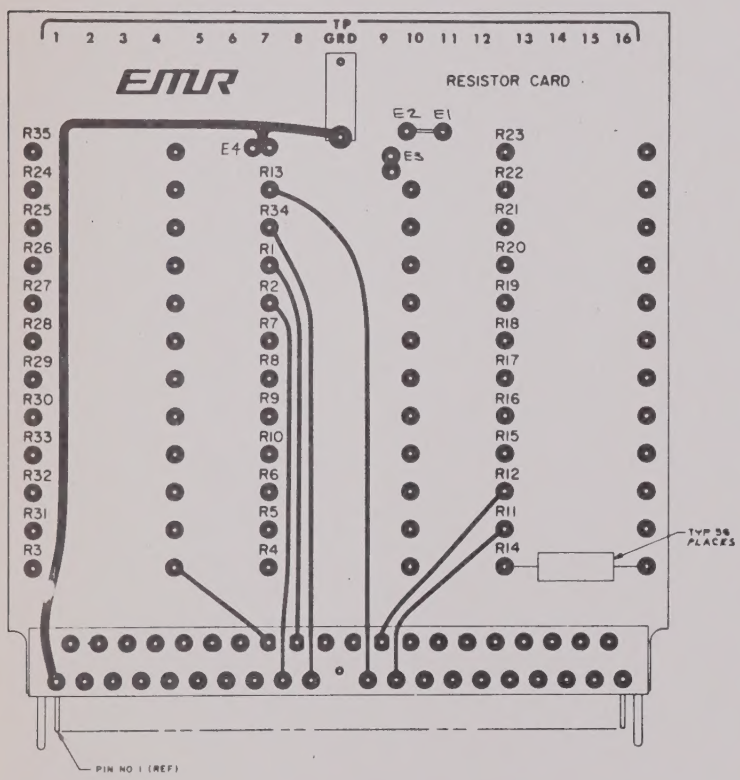
Parts List

Figure 1 (Sheet 3 of 3)

EMR PART NO. 8301
RESISTOR CARD

The Resistor Card provides current sources for interface purposes and resistive loads for front-panel switches and internal logic gates.

Eight different configurations of the card (8301-1 thru -8) are available by use of jumper wires between "E" terminals and use of different resistor values. These various configurations are reflected in Table 1 shown below.



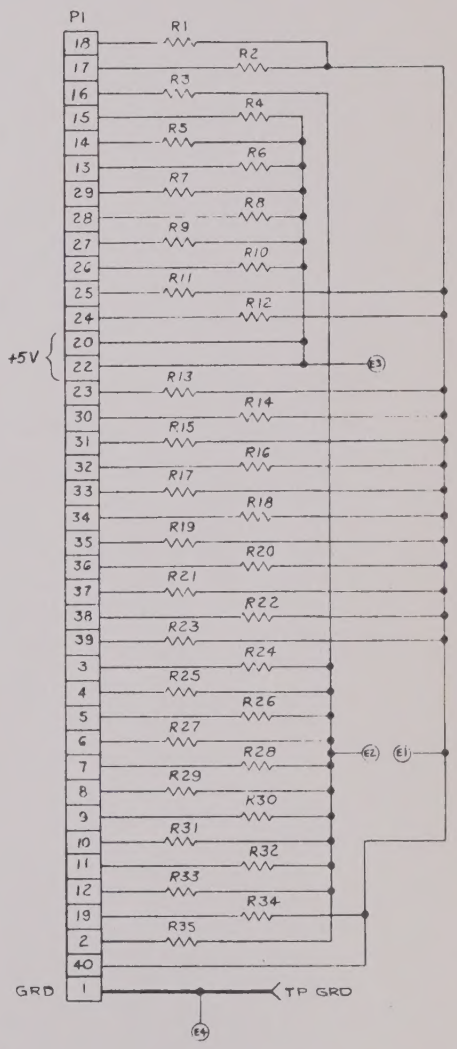


TABLE 1		
DASH NO.	COMPONENT VALUE (±10%, 1/2W)	"E" CONNECTIONS
Basic	R1 thru R35 - 1.6K	E1 to E2
-1	R1 thru R35 - 16K ±5%, 1/2W	E1 to E2
-2	R1 thru R35 - 6.8K	E1 to E2
-3	R4 thru R10 - 10K; R1, 2, 3, R11 thru R35 - 22K	E1 to E2
-4	R4, 5, 6, 9, 10 - 680Ω; R7, 8 - 270Ω; R1, 2, 3, R11 thru R35 - 22K	E1 to E2
-5	R3, R24 thru R33, &35 - 22K; R1, 2, R4 thru R23, & 34 - 10K	E2 to E4
-6	R1, 3, 13, 14, 16, 18, 29, 32, & 33 - 47M; R2, 4 thru 12, 15, 17, 19 thru 28, 30, 31, 34, & 35 - 1.6K	E1 to E2
-7	R1, 2, 3, 11 thru 34 - 91Ω; R4 thru R10 - 1.6K; R35 - 2.2K	E1 to E4 & E2 to E4
-8	R1, 2, R11 thru R23, & R34 - 1.6K; R3 thru R10, R24 thru R33, & R35 - 270Ω	E1 to E2 to E3

NOTES:

1. Unless otherwise specified, all resistor values are in ohms (K=1000) 10%, 1/4W.
2. On -7 and -8 configurations, all resistors are 5%, 1/4W.

Revised: 12-18-68